13" Intel TGL-UP3
Platform Block Diagram

QUANTA X3A

	PROJECT : X3AC Quanta Computer Inc.	
Size	Document Number Power EMI	Rev 3A
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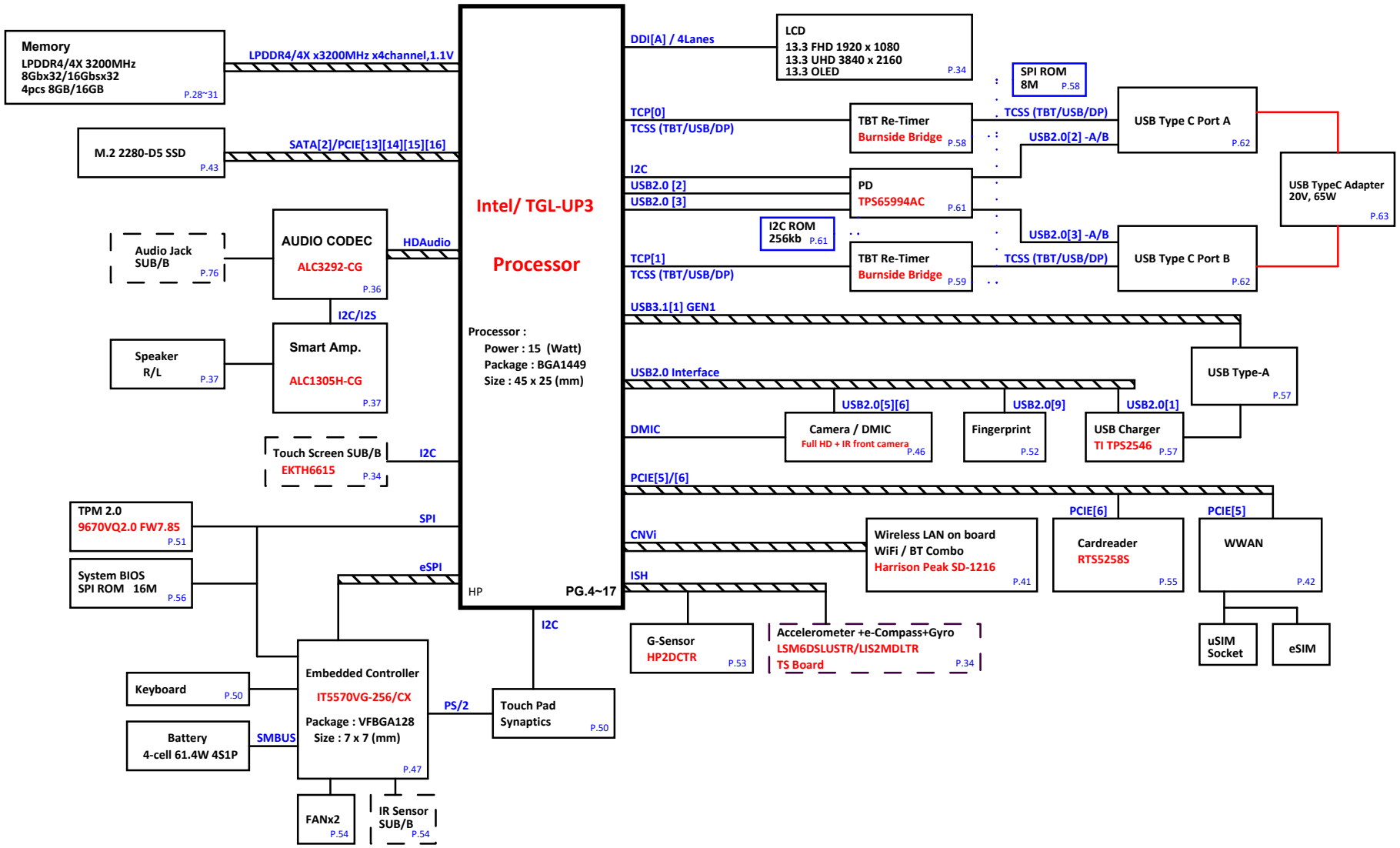

PROJECT : X3AC

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Intel Block Diagram	3A

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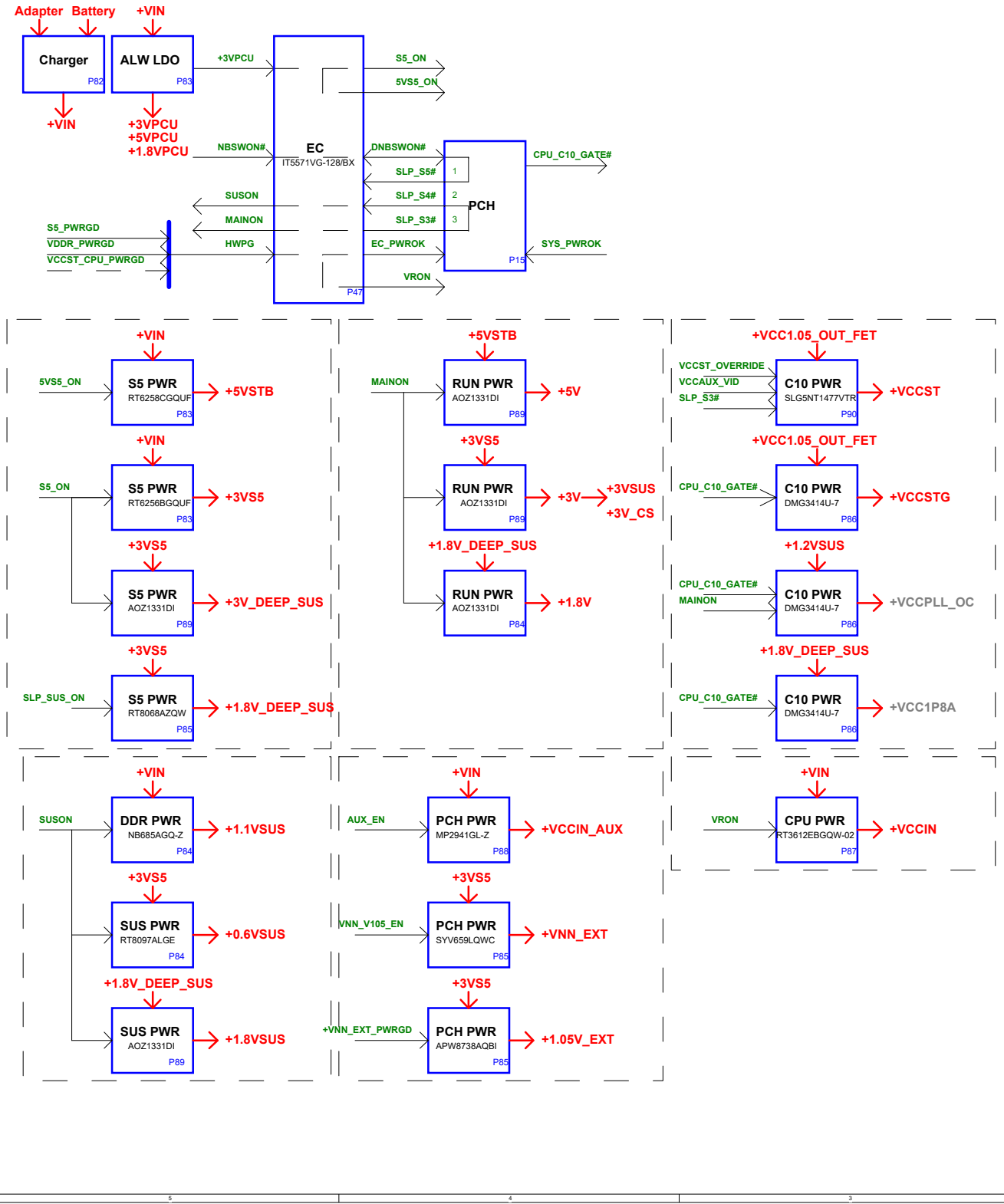
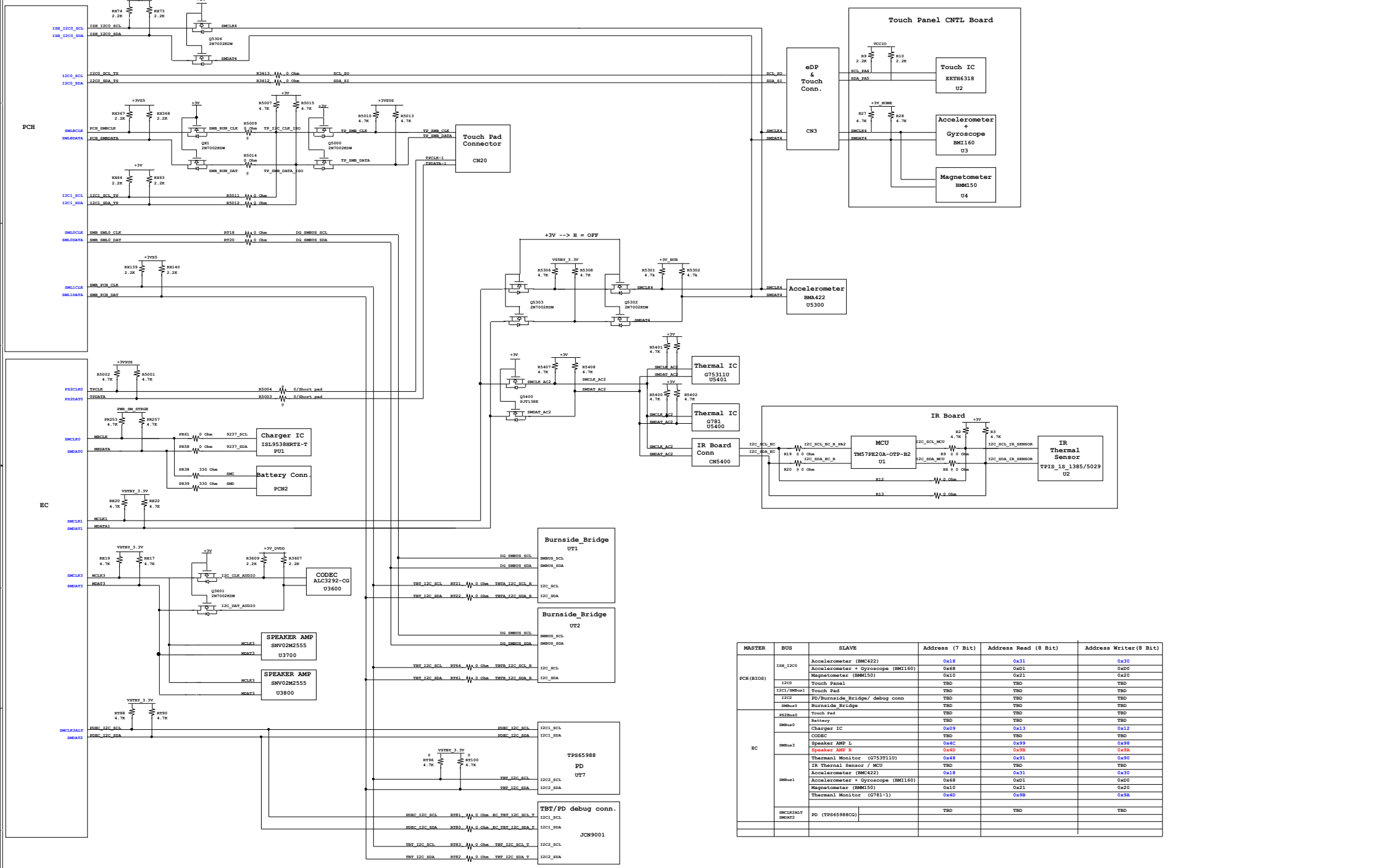


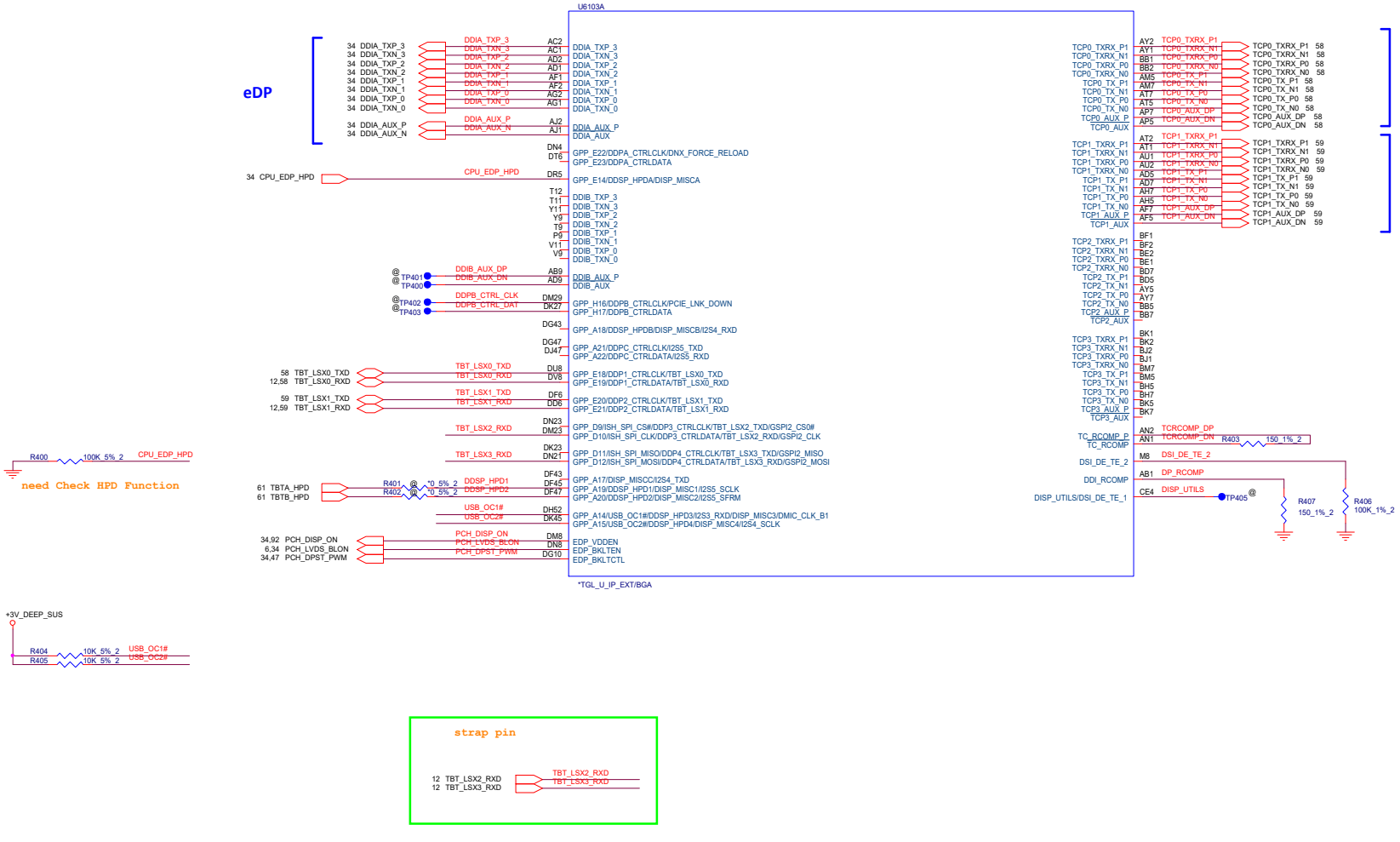
Main Power Rails

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+3V_WLAN_P	+3.3V	WLAN Power	CNVI_EN#	
+1.8VSUS	+1.8V	LPDDR4/4X Suspend Power	SUSON	
+0.6VSUS	+0.6V	LPDDR4/4X Suspend Power	SUSON	
+1.05V_EXT	+1.05V	PCH Power	+VNN_EXT_PWRGD	
+VNN_EXT	+1.05V	PCH Power	VNN_V105_EN	
+1.1VSUS	+1.1V	LPDDR4/4X Suspend Power	SUSON	
+1.8V	+1.8V	Audio Codec power	MAINON	
+1.8V_DEEP_SUS	+1.8V	PCH power	SLP_SUS_ON	
+3V	+3.3V	3V Run Power	MAINON	
+3VSUS	+3.3V	3V Suspend Power	MAINON	
+3VS5	+3.3V	3V S5 Power	S5_ON	
+3VPCU	+3.3V	3V Always Power	+VIN	
+5V	+5V	5V Run Power	MAINON	
+5VSTB	+5V	5V S5 Power	5VS5_ON	
+5VPCU	+5V	5V Always Power	+VIN	
+VCCIN_AUX	+1.8V	PCH Power	AUX_EN	
+VCCIN	SVID +1.89V(MAX)	CPU Core Power	VRON	
+VIN	+19V	AC power input		



MASTER	BUS	SLAVE	Address (7 Bit)	Address Read (8 Bit)	Address Writer(8 Bit)
PCH(BIOS)	ISH_I2C0	Accelerometer (BMC422)	0x18	0x31	0x30
		Accelerometer + Gyroscope (BMI160)	0x68	0x01	0x00
		Magnetometer (BMM150)	0x10	0x21	0x20
	I2C0	Touch Panel	TBD	TBD	TBD
	I2C1/SMBus1	Touch Pad	TBD	TBD	TBD
	I2C2	PD/Burnside_Bridge/ debug conn	TBD	TBD	TBD
	SMBus0	Burnside_Bridge	TBD	TBD	TBD
EC	PS2Bus0	Touch Pad	TBD	TBD	TBD
	SMBus0	Battery	TBD	TBD	TBD
		Charger IC	0x09	0x13	0x12
	SMBus3	CODEC	TBD	TBD	TBD
		Speaker AMP L	0x4C	0x99	0x98
		Speaker AMP R	0x4D	0x9B	0x9A
	SMBus1	Thermanl Monitor (G753T11U)	0x48	0x91	0x90
		IR Thermal Sensor / MCU	TBD	TBD	TBD
		Accelerometer (BMC422)	0x18	0x31	0x30
		Accelerometer + Gyroscope (BMI160)	0x68	0xD1	0xD0
		Magnetometer (BMM150)	0x10	0x21	0x20
		Thermanl Monitor (G781-1)	0x4D	0x9B	0x9A
	SMCLK2ALT SMDAT2	PD (TPS65988CG)	TBD	TBD	TBD

PROJECT : X3AC
Quanta Computer Inc.



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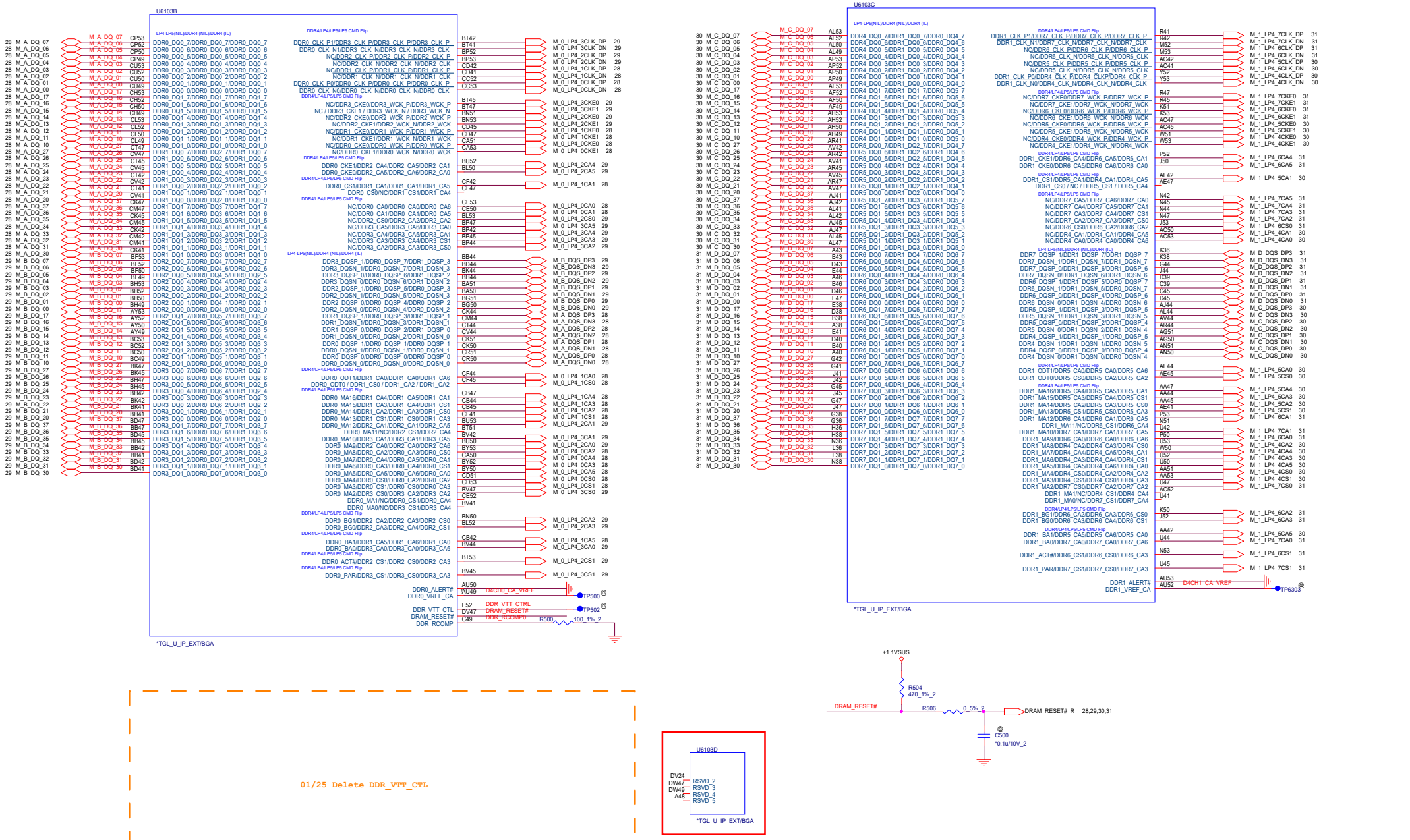
TIGER LAKE Processor LPDDR4/4X



PROJECT : X3AC	
Quanta Computer Inc.	
Size	Document Number: TGL-U 2/14 (LPDDR4 I/F) — Rev: 3A
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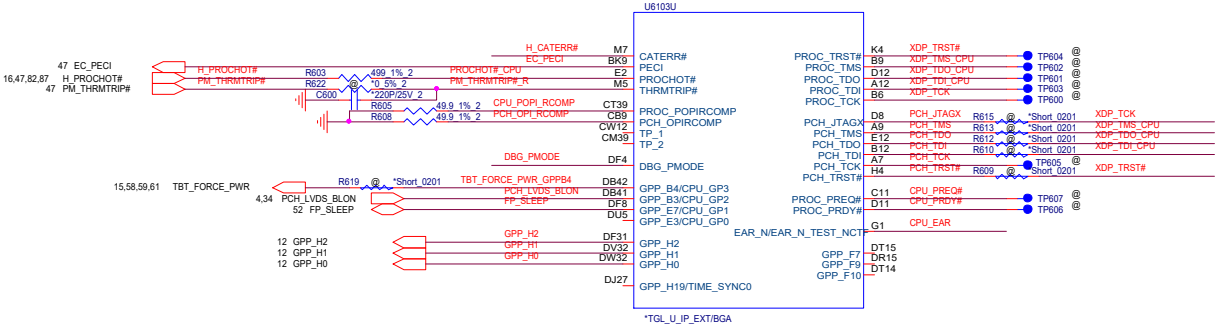
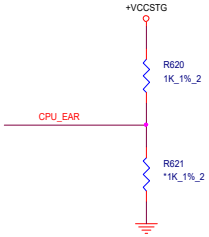
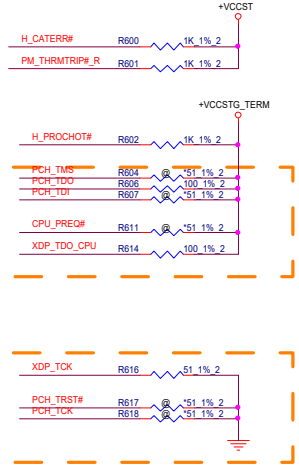




Strap pin

12 DBG_PMODE — DBG_PMODE



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Size: Custom	Document Number: TGL-U 3/14 (CPU MISC/JTA)	Rev: 3A
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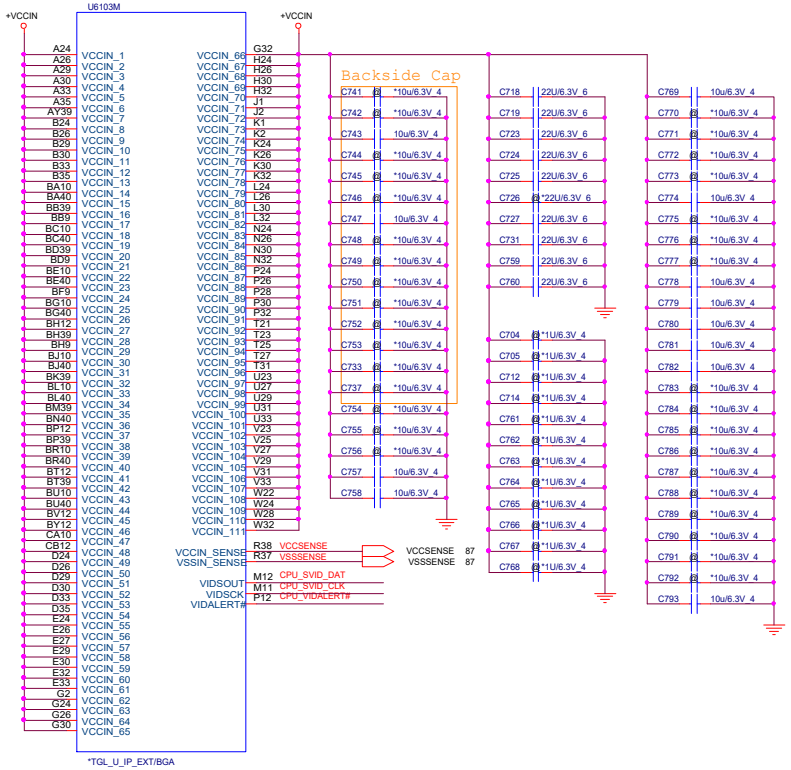
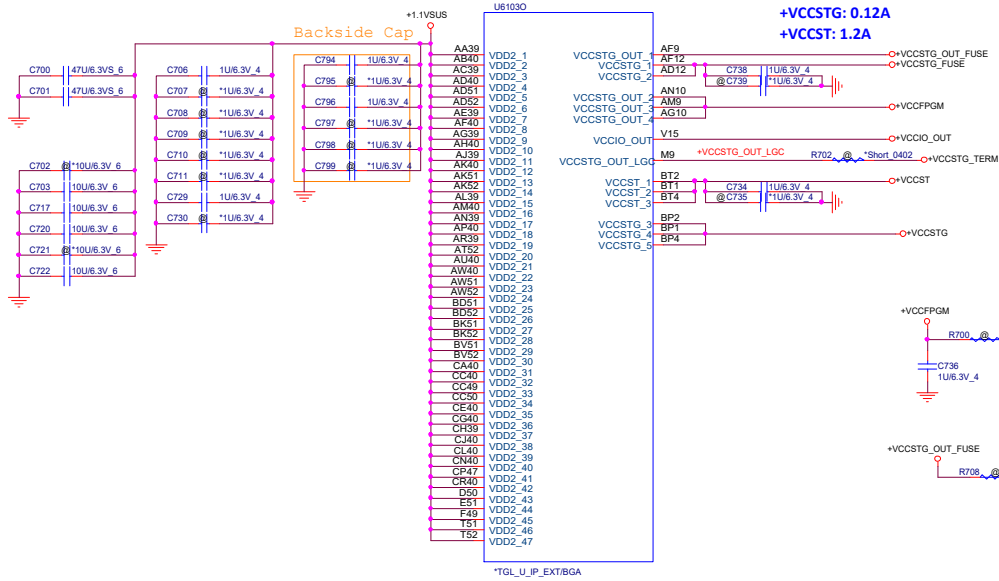
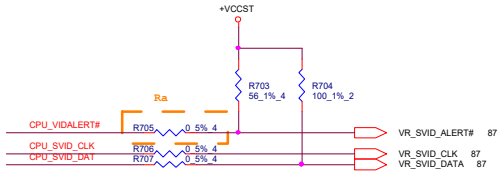
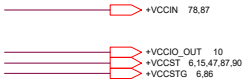
+VCCIN: 70A









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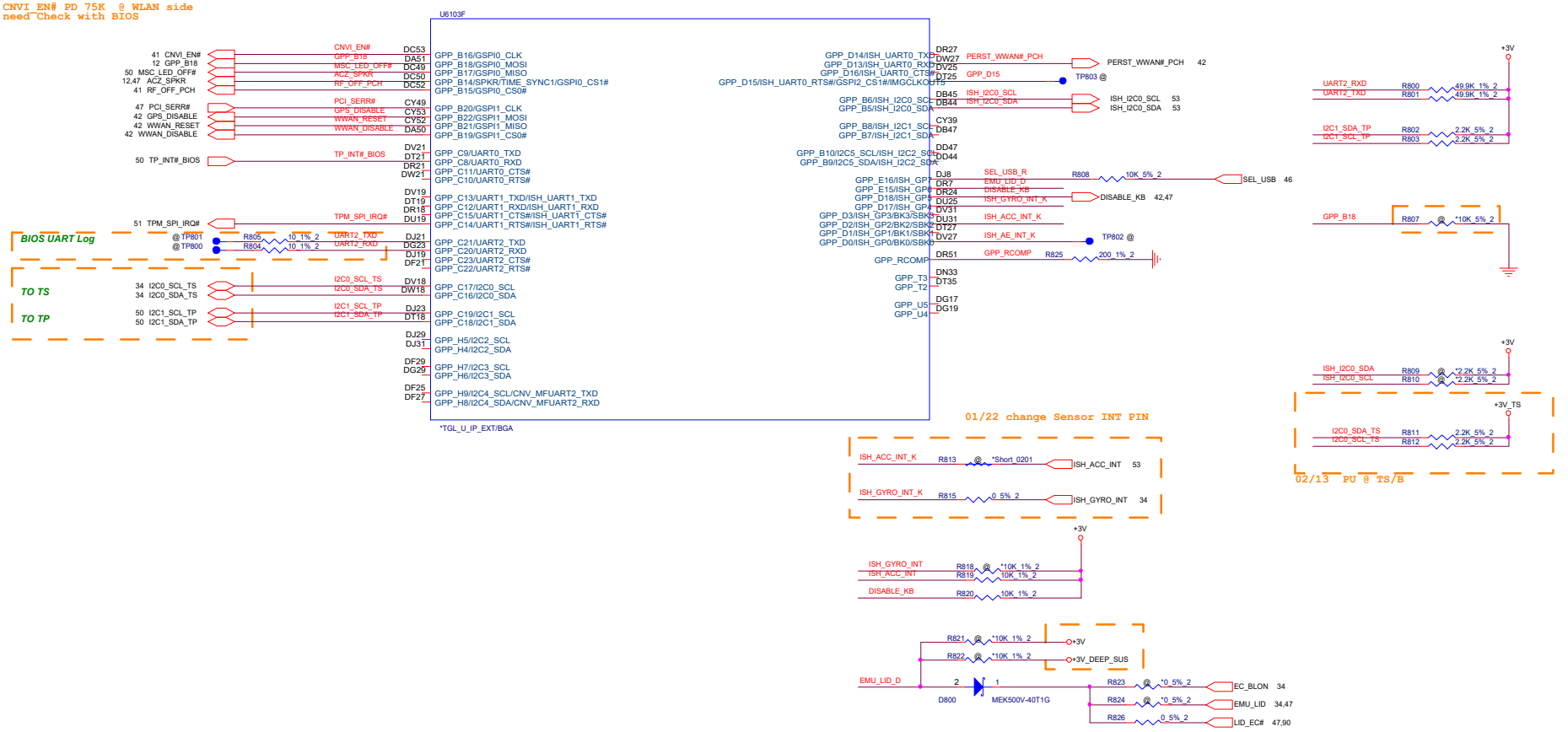
01/17 Add SOC_ENBKL for S5 Turn off the Backlight

CNVI_EN# PD 75K @ WLAN side need Check with BIOS



PROJECT : X3AC Quanta Computer Inc.			
Size: Custom	Document Number: TGL-U 5/14 (I2C/ISH)		Rev: 3A
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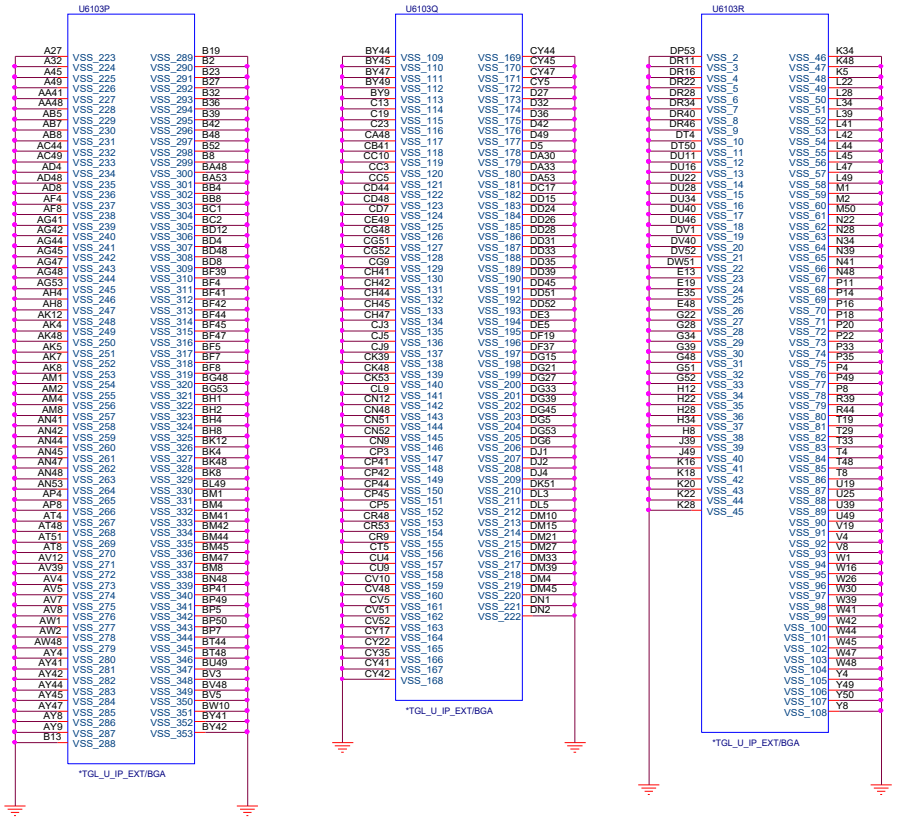
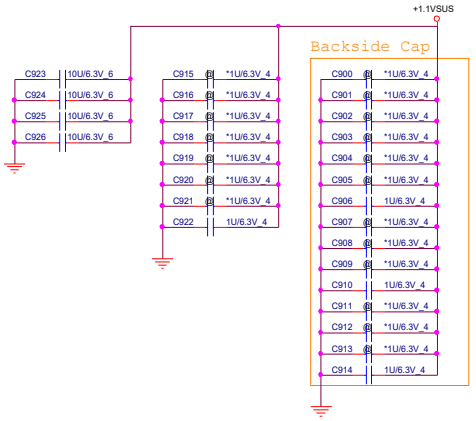


+1.1VSUS POWER CAP MOVE FROM PAGE 7



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Quanta Computer Inc.

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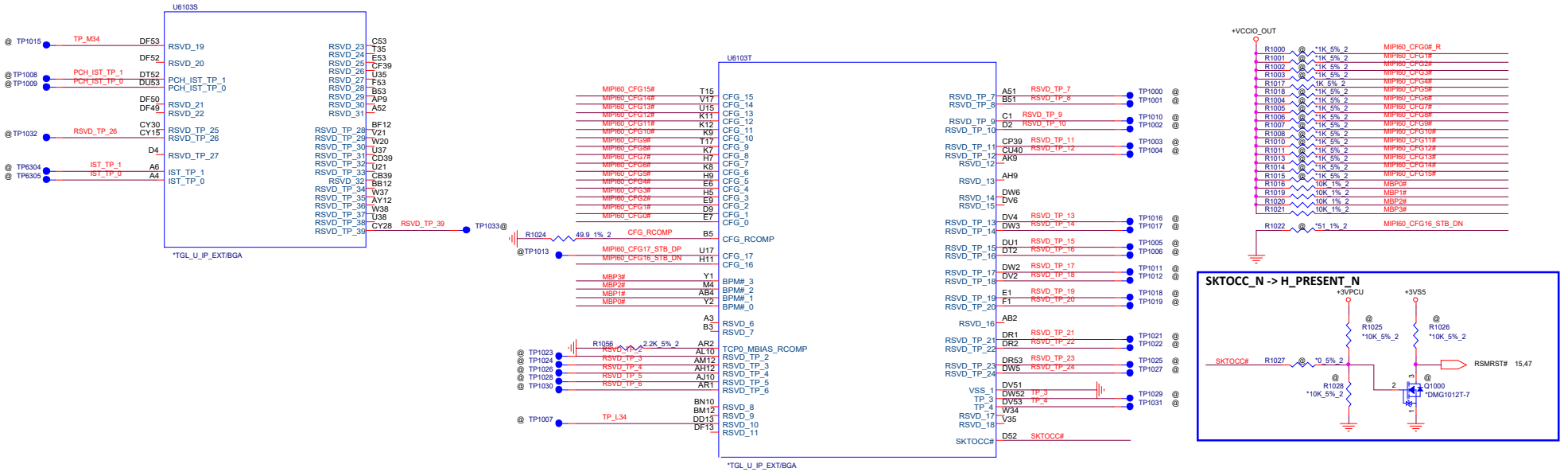
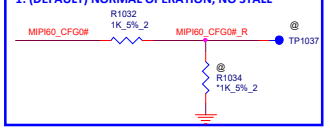


EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

CFG0

1: (DEFAULT) NORMAL OPERATION; NO STALL

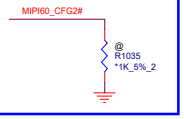


PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2

1: (DEFAULT)NORMAL OPERATION

0: LANE REVERSAL



PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

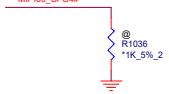
CFG4

1: DISABLED

AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

0: ENABLED

NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

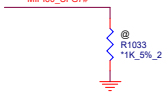


PEG DEFER TRAINING

CFG7

1: (DEFAULT) PEG TRAIN IMMEEDIATELY FOLLOWING XXRESETB DEASSERTION

0: PEG WAIT FOR BIOS FOR TRAINING

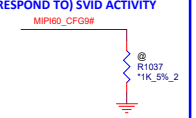


NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT

0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

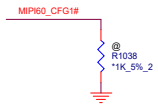


PCH/ PCH LESS MODE SELECTION

CFG1

1: (DEFAULT) NORMAL OPERATION

0: PCH-LESS MODE



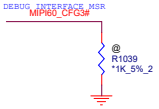
PHYSICAL_DEBUG_ENABLED(DFX PRIVACY)

CFG3

1: DISABLED

0: ENABLED

SET DFX ENABLED BIT IN DEBUG_INTERFACE_MSR



PCIE PORT BIFURCATION STRAPS

CFG[6:5]

11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED

01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED

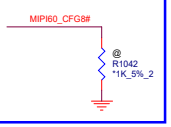
00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

ALLOW THE USE OF NOA ON LOCKED UNITS

CFG8

1: DISABLED(DEFAULT): IN THIS CASE, NOA WILL BE DISABLE IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

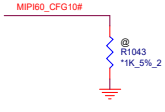


SAFE MODE BOOT

CFG10

1: POWER FEATURES ACTIVATED DURING RESETT

0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

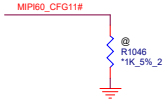


DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT

CFG11

1:(DEFAULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED

0: DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

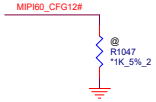


PM SYNC LEGACY

CFG12

1: (DEFAULT) PMSYNC 2.0

0: LEGACY

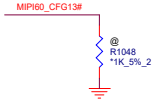


PMSYNC AYNC MODE- PM SYNC

CFG13

1: (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)

0: ASYNC - 4-24MHZ CYCLES PER BIT



PROJECT : X3AC

Quanta Computer Inc.

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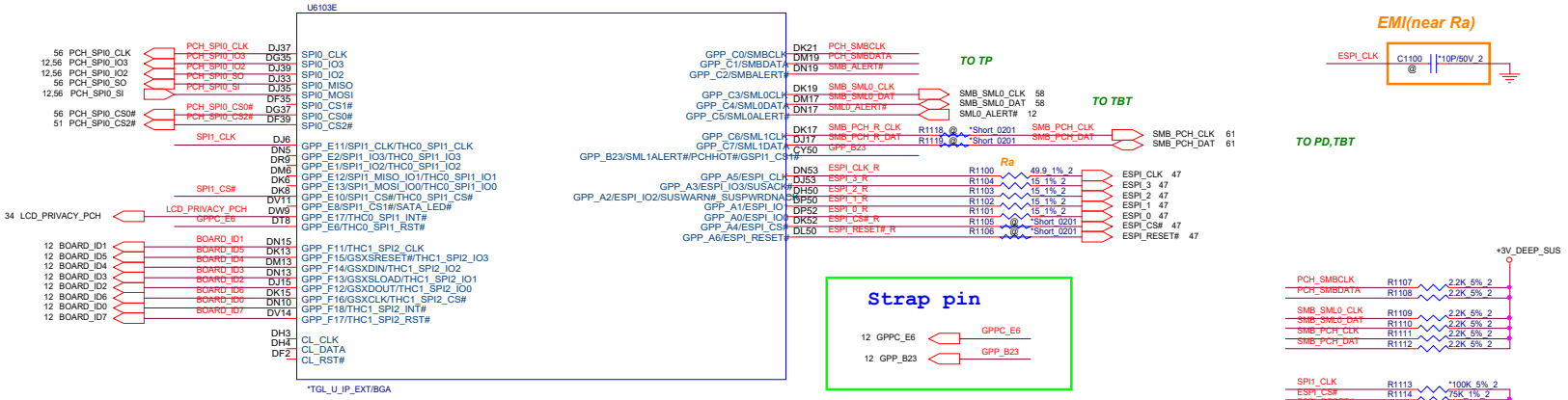

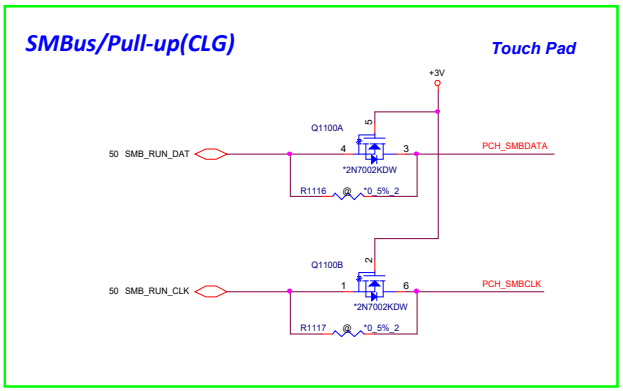

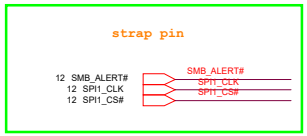

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Quanta Computer Inc.	
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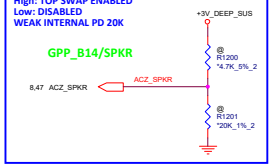
TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

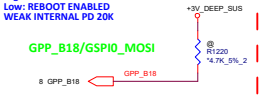
GPP_B14/SPKR



NO REBOOT

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

GPP_B18/GSPI0_MOSI

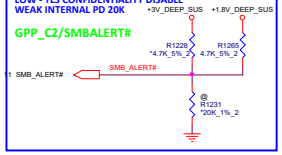


01/15 PD 10K at PAGE.8

TLS CONFIDENTIALITY

High - TLS CONFIDENTIALITY ENABLE
LOW - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

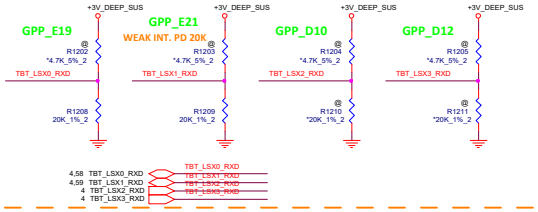
GPP_C2/SMBALERT#



TBT LSX PINS VCCIO CONFIGURATION

High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD

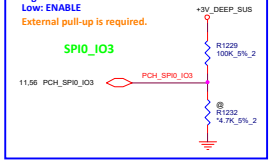
GPP_E19 GPP_E21 (WEAK INT. PD 20K) GPP_D10 GPP_D12



(RSVD) A0 PERSONALITY STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

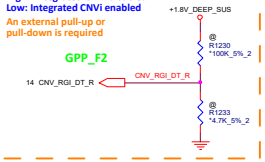
SPI0_IO3



M.2 CNVi Mode Select

High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required

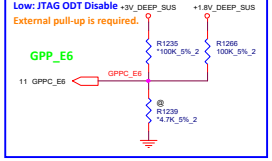
GPP_F2



(RSVD) JTAG ODT DISABLE

High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

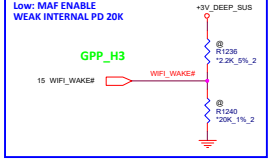
GPP_E6



MAF/SAF STRAP

High: SAF ENABLE
Low: MAF ENABLE
WEAK INTERNAL PD 20K

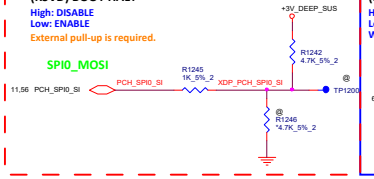
GPP_H3



(RSVD) BOOT HALT

High: DISABLE
Low: ENABLE
External pull-up is required.

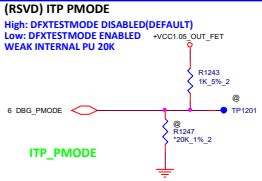
SPI0_MOSI



(RSVD) ITP PMODE

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

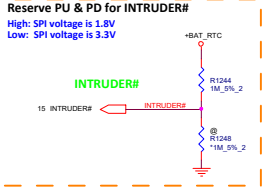
ITP_PMODE



Reserve PU & PD for INTRUDER#

High: SPI voltage is 1.8V
Low: SPI voltage is 3.3V

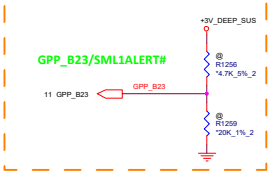
INTRUDER#



CPUNSSC CLOCK FREQ

High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

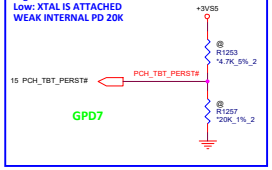
GPP_B23/SML1ALERT#



(RSVD) XTAL INPUT MODE

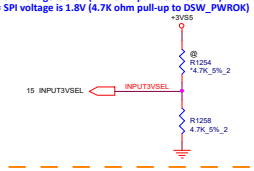
High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

GPD7



STRAP FOR SPI 1.8V/3.3V SELECTION

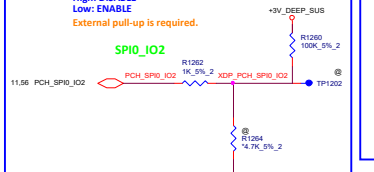
0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)



(RSVD) CONSENT STRAP

High: DISABLE
Low: ENABLE
External pull-up is required.

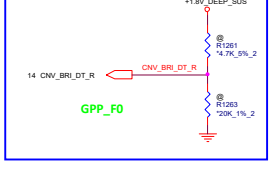
SPI0_IO2



XTAL FREQUENCE SEL

High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

GPP_F0



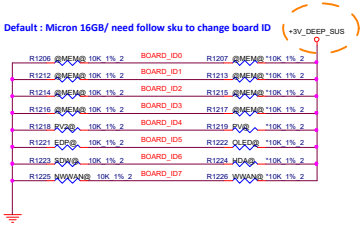
RING OSCILLATOR BYPASS

High: BYPASS MODE ENABLED
Low: RING OSCILLATOR
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_H3

WWAN=1	SdW=0	Non-OLED=0	PV2=0	DDR memory board ID							
WIFI=0	HDA=1	OLED=1	PV=1								
Board ID7	Board ID6	Board ID5	Board ID4	Board ID3	Board ID2	Board ID1	Board ID0	Board ID	Vendor Part Number	QCI P/N	QCI P/N (TOP)
GPP_G7	GPP_G6	GPP_G5	GPP_G4	GPP_G3	GPP_G2	GPP_G1	GPP_G0	GPIO			
0	0	0	0	0	0	0	0	Micron/8G	MT53E512M32D2NP-046 WT:E	AKD5SZUTL03	AKD5SZUTL02
0	0	0	0	0	0	0	1	Hynix/8G	H9HCNNNBKMALHR-NEE	AKD5RG0TW21	AKD5RG0TW23
0	0	0	0	0	0	1	0	Samsung/8GB	K4U6E3S4AM-MGCJ		AKD5RZST539
0	0	0	0	0	0	0	1	Micron/16G	MT53E1G32D4NQ-046 WT:E	AKD5SWDTL14	AKD5SWDTL11
0	0	0	0	0	1	0	0	Hynix/16G	H9HCNNNCPMALHR-NEE	AKD5SGUTW04	AKD5SGUTW03
0	0	0	0	0	1	0	1	Samsung/8GB	K4U6E3S4AA-MGCL	AKD5MZST519	AKD5MZST520
0	0	0	0	0	1	1	0	Samsung/16GB	K4UBE3D4AA-MGCL	AKD5PZST538	AKD5PZST539
0	0	0	0	0	1	1	1	New Hynix/8G	H9HCNNNBKMMLXR-NEE	AKD5RG0TW34	AKD5RG0TW36
0	0	0	0	1	0	0	0	New Samsung/8G	K4U6E3S4AA-MGCR	AKD5MZST530	AKD5MZST534
0	0	0	0	1	0	0	1	New Hynix/16G	H9HCNNNCPMMLXR-NEE	AKD5SG0TW07	AKD5SG0TW09
0	0	0	0	1	0	1	0	New Micron/16G	MT53E1G32D2NP-046 WT:A	AKD5SWDTL20	AKD5SWDTL21
0	0	0	0	1	0	1	1	New Samsung/16G	K4UBE3D4AA-MGCR	AKD5PZST551	AKD5PZST554
0	0	0	0	1	1	0	0	Reserve			
0	0	0	0	1	1	0	1	Reserve			
0	0	0	0	1	1	1	0	Reserve			
0	0	0	0	1	1	1	1	Reserve			

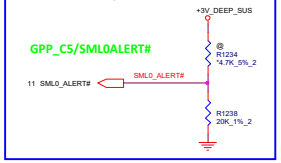
Default : Micron 16GB/ need follow sku to change board ID



Boot Strap 0

WEAK INTERNAL PD 20K

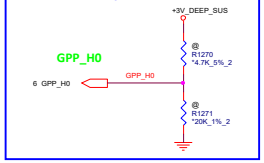
GPP_C5/SML0ALERT#



Boot Strap 1

WEAK INTERNAL PD 20K

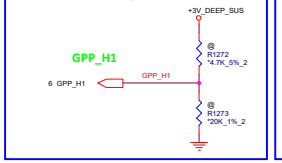
GPP_H0



Boot Strap 2

WEAK INTERNAL PD 20K

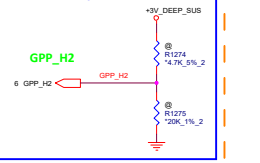
GPP_H1



Boot Strap 3

WEAK INTERNAL PD 20K

GPP_H2



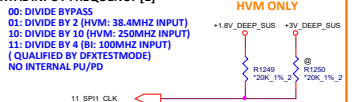
Boot Strap	4-bit boot strap configuration encodings
0000	BIOS/CSME on SPI & eSPI is enabled
0010	BIOS/CSME on SPI & eSPI is disabled
0100	BIOS on eSPI Peripheral Channel; CSME on master SPI
1000	BIOS/CSME on eSPI
1100	BIOS on eSPI peripheral Channel; CSME on slave SPI

XTAL INPUT FREQUENCY [1]

00: DIVIDE BYPASS
01: DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10: DIVIDE BY 10 (HVM: 250MHZ INPUT)
11: DIVIDE BY 4 (BI: 100MHZ INPUT)
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

HVM ONLY

GPP_E11

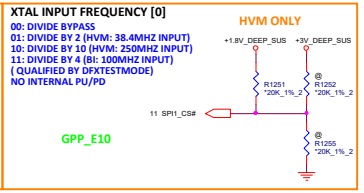


XTAL INPUT FREQUENCY [0]

00: DIVIDE BYPASS
01: DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10: DIVIDE BY 10 (HVM: 250MHZ INPUT)
11: DIVIDE BY 4 (BI: 100MHZ INPUT)
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

HVM ONLY

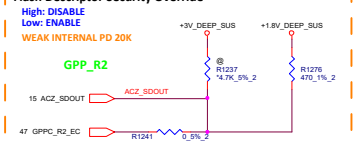
GPP_E10



Flash Descriptor Security Override

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

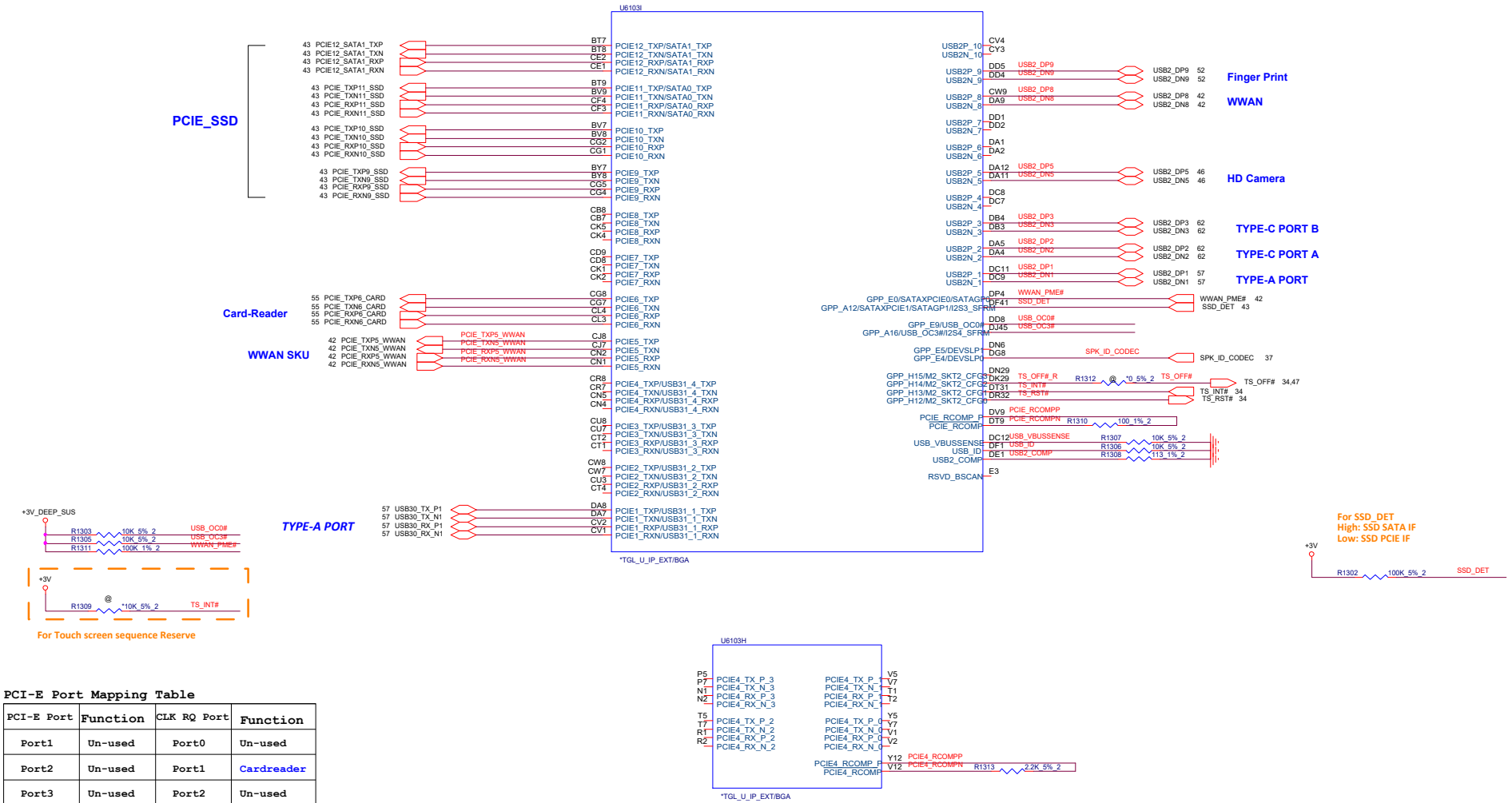
GPP_R2



PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TGL-U 9/14 (HW STRAP)	3A

Date: Wednesday, October 07, 2020 Sheet 12 of 57



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	Cardreader
Port3	Un-used	Port2	Un-used
Port4	Un-used	Port3	Un-used
Port5	WWAN	Port4	WWAN
Port6	Cardreader	Port5	SSD HDD
Port7	Un-used		
Port8	Un-used		
Port9	Un-used		
Port10	Un-used		
Port11	Un-used		
Port12	Un-used		
Port13	SSD HDD		
Port14	SSD HDD		
Port15	SSD HDD		
Port16	SSD HDD		

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.1_GEN2_MB-1
PORT-2	TYPEC-A
PORT-3	TYPEC-B
PORT-4	NC
PORT-5	HD Camera
PORT-6	IR Camera
PORT-7	NC
PORT-8	WWAN
PORT-9	Finger Print
PORT-10	NC

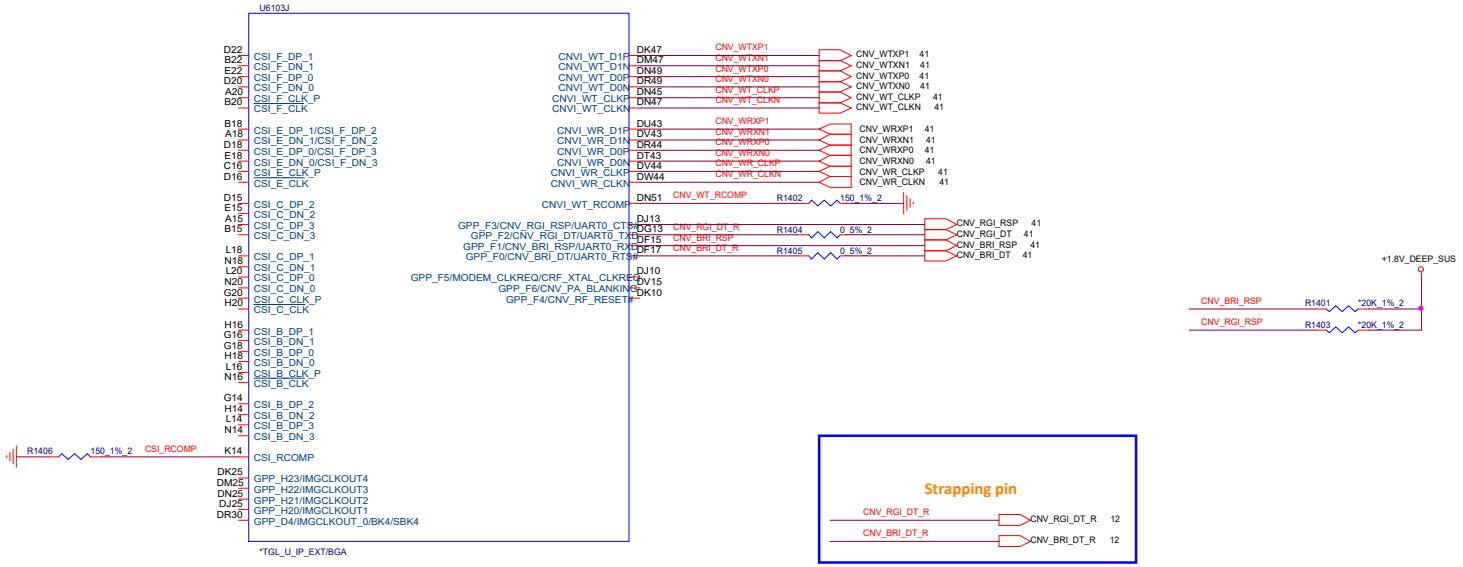
USB3.0 Port Mapping Table

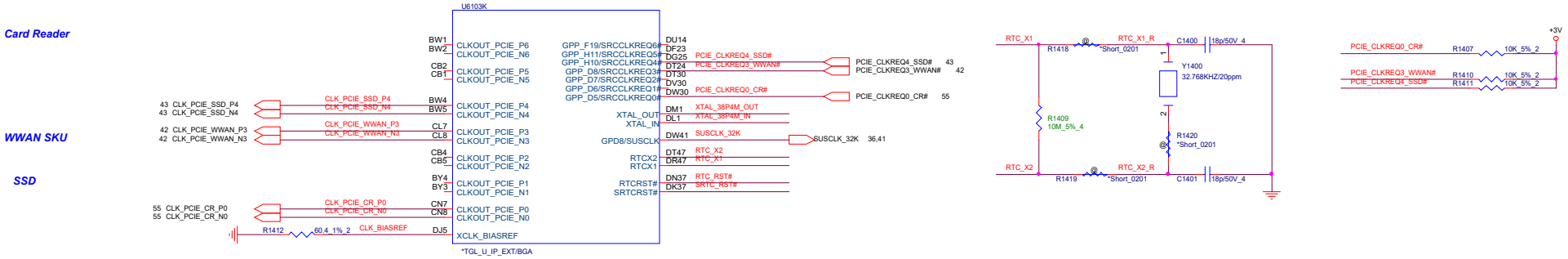
USB3.0	Function
PORT-1	USB3.1_GEN2_MB-1
PORT-2	NC
PORT-3	NC
PORT-4	For DCI Debug (INTEL)

PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TGL-U 10/14(USB/PCIE/SAT)	3A

Date: Wednesday, October 07, 2020 Sheet 13 of 57





Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

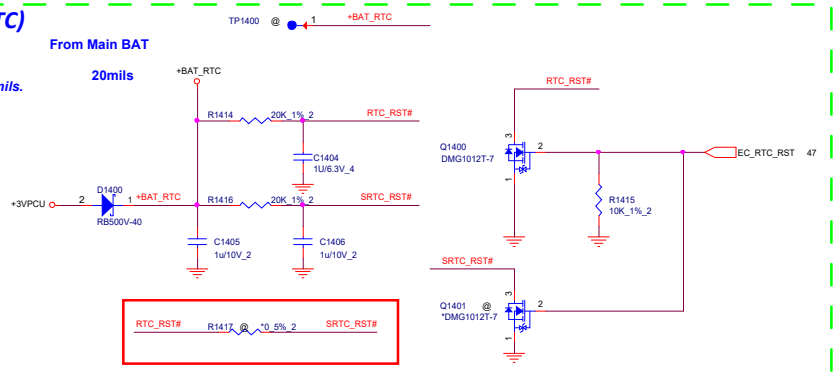
RTC Clock 32.768KHz

RTC Circuitry(RTC)

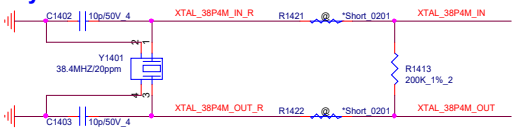
From Main BAT

20mils

RTC Power trace width 20mils.



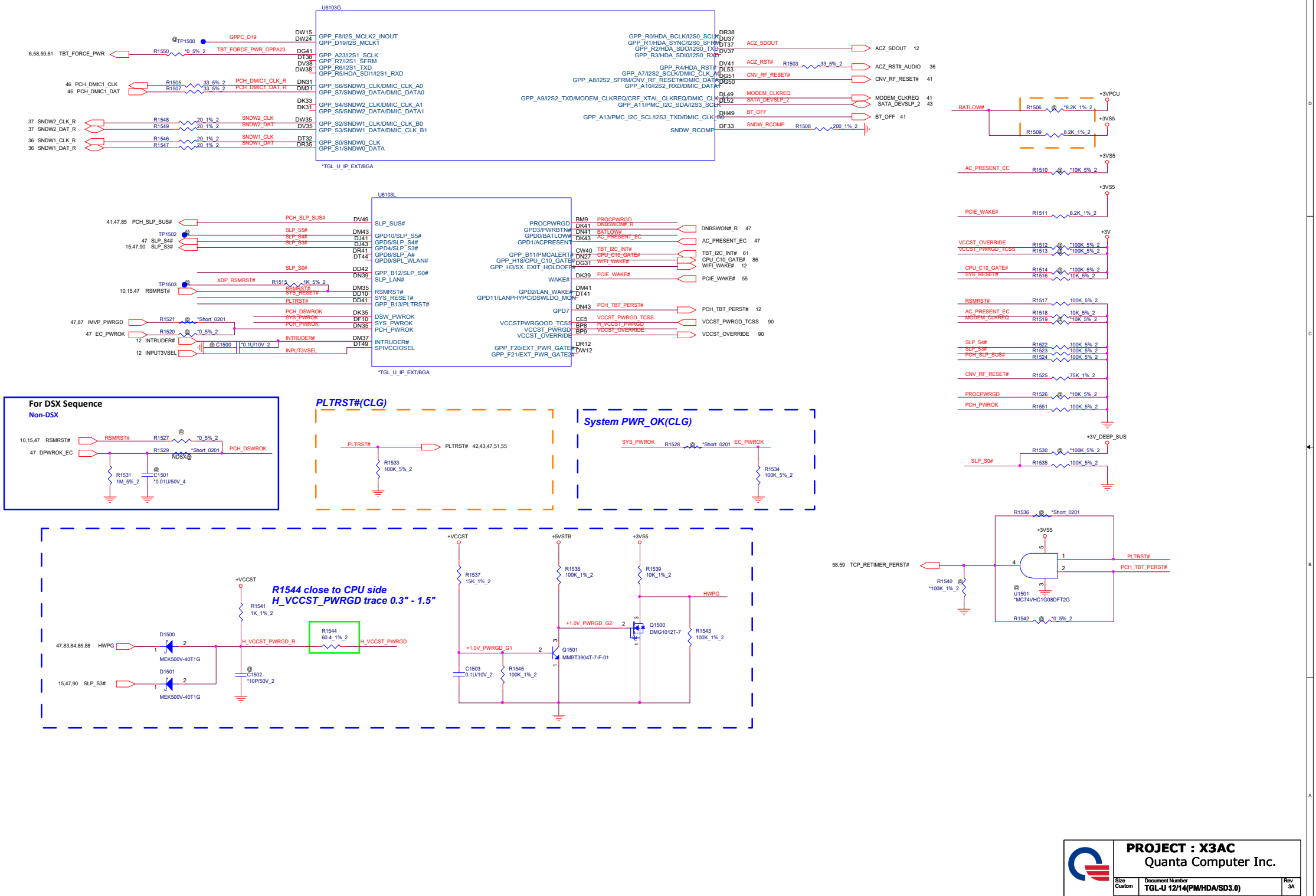
Crystal 38.4MHz



SI2 Del R532,Q24

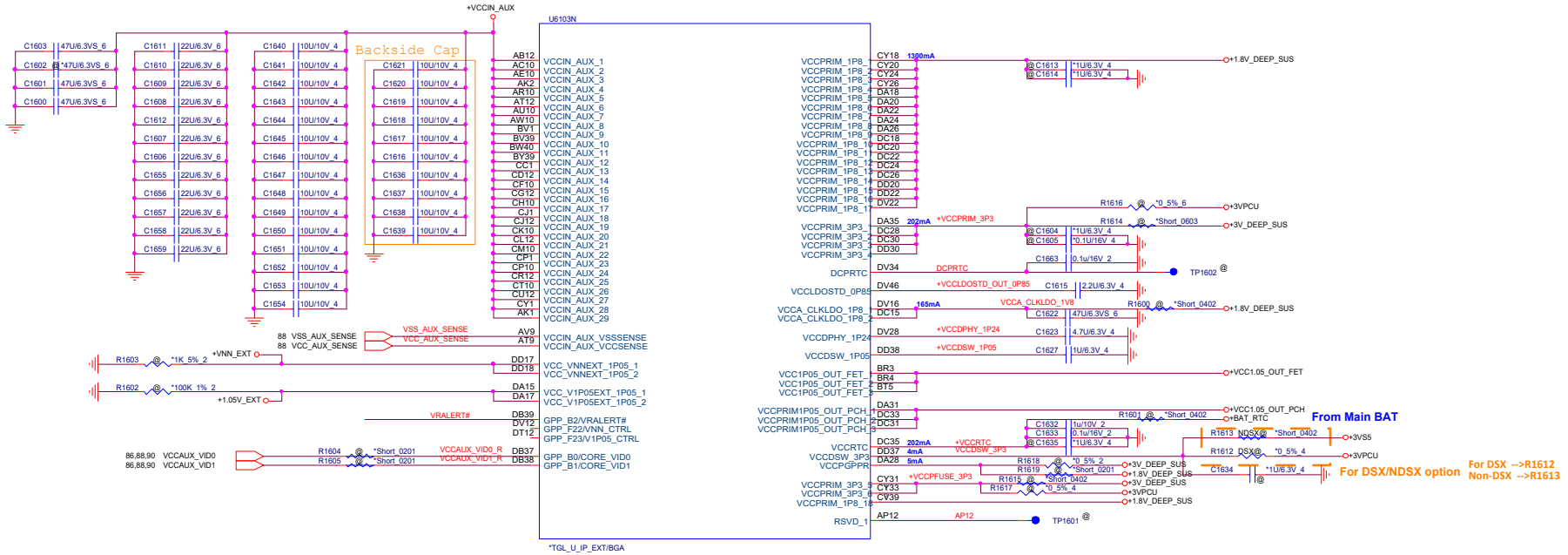
PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TGL-U 11/14(CSI/CNVI/CLK)	3A
Date: Wednesday, October 07, 2020	Sheet 14 of 57	

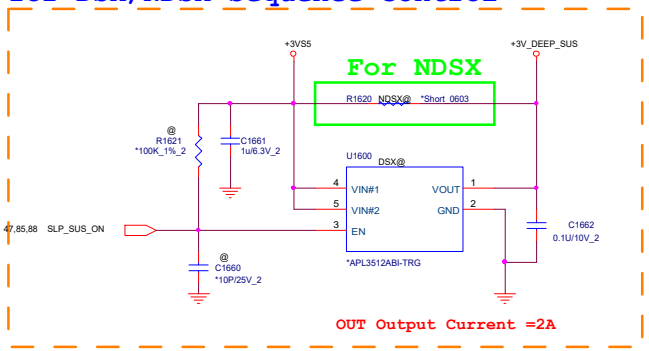


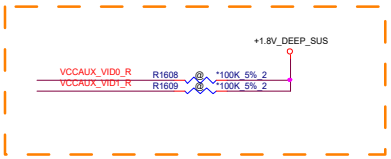
PROJECT : X3AC	
Quanta Computer Inc.	
Size: Custom	Document Number: TGL-U 12/14(PM/HDA/SD3.0)
Rev: 3A	
Date: Wednesday, October 07, 2020	Sheet 15 of 57

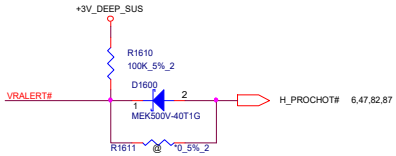
+VCCIN_AUX: 32A



for DSX/NDSX Sequence Control



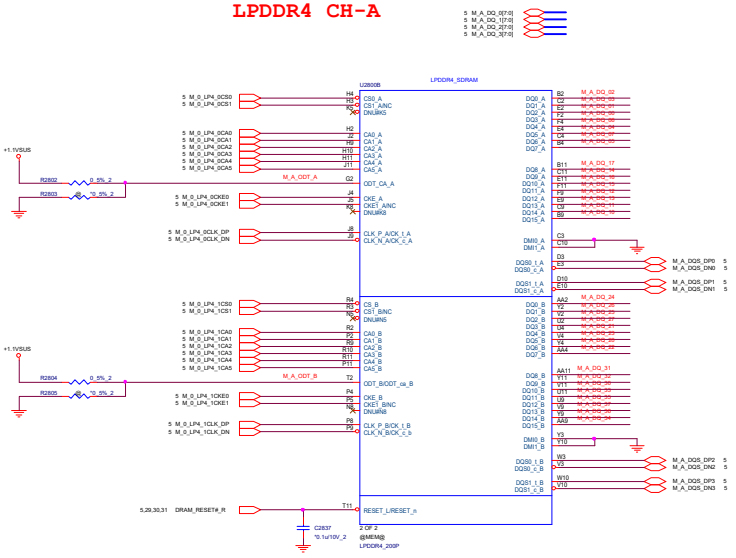


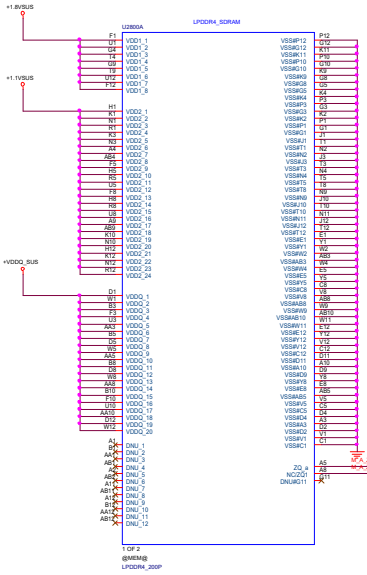


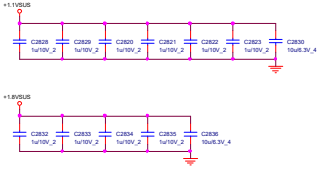
PROJECT : X3AC	
Quanta Computer Inc.	
Size: Custom	Document Number: TGL-U 13/14(PCH POWER)
Rev: 3A	
Date: Wednesday, October 07, 2020	Sheet 16 of 57

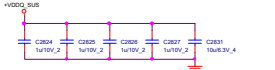
Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

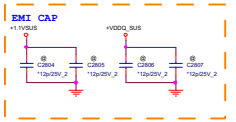
LPDDR4 CH-A

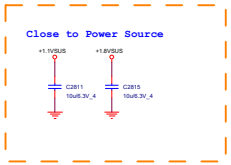


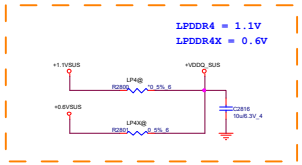










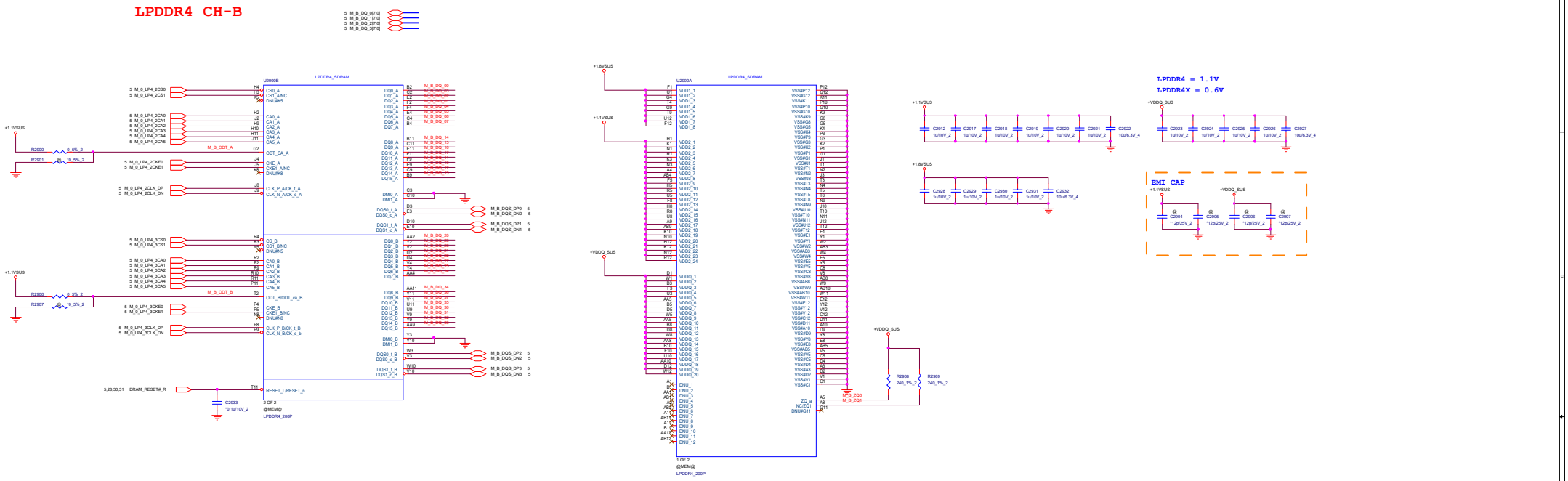


EEPROM

PROJECT : X3AC	
Quanta Computer Inc.	
Size	Document Number: MEMORY_A_LPDDR4 — Rev: 3A
Date: Wednesday, October 07, 2020	Sheet 17 of 57

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

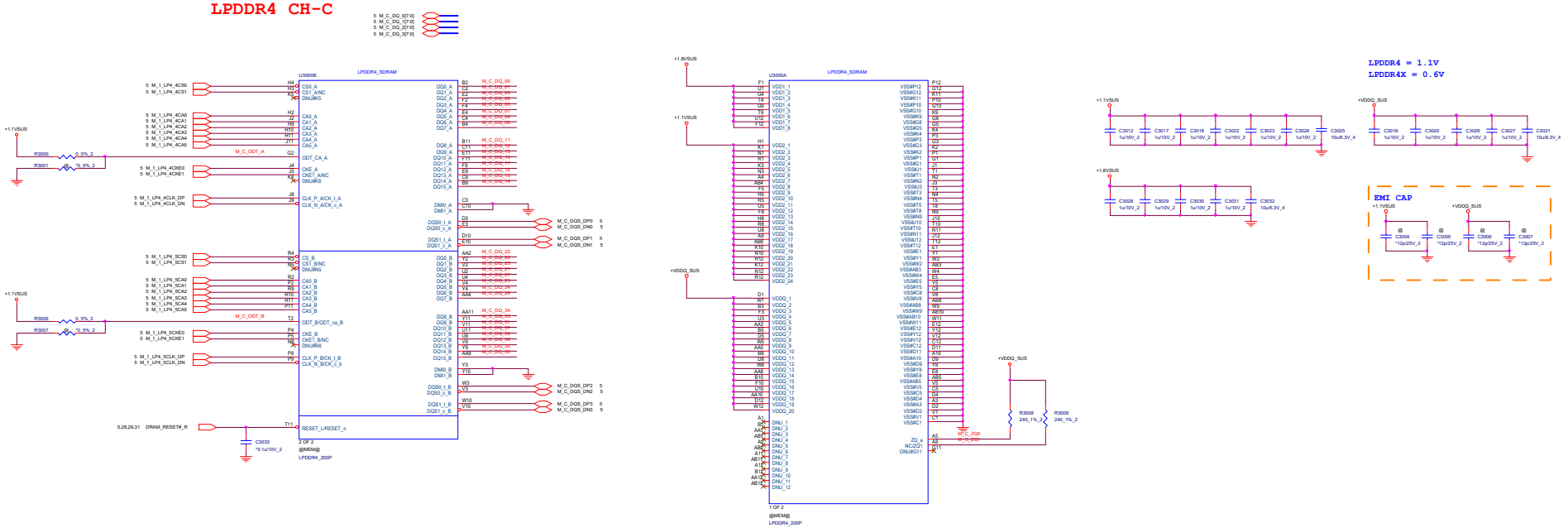
LPDDR4 CH-B



PROJECT : X3AC	
Quanta Computer Inc.	
Size	Document Number: MEMORY_B_LPDDR4 — Rev: 3A
Date: Wednesday, October 07, 2020	Sheet 18 of 57

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

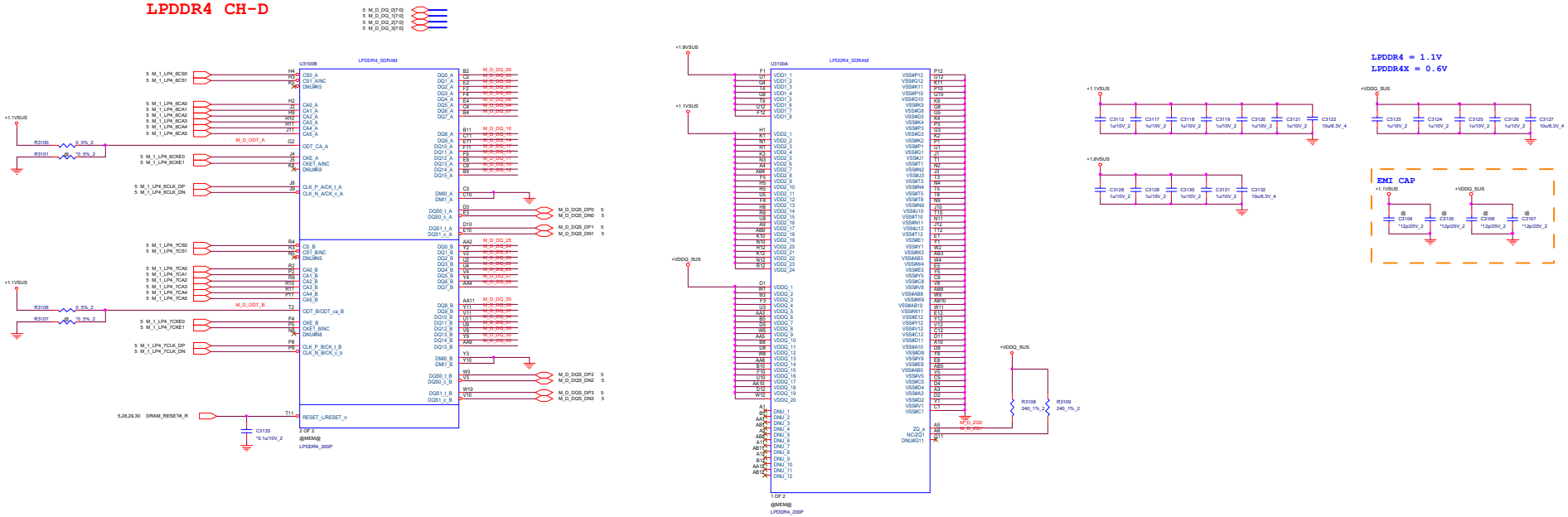
LPDDR4 CH-C



PROJECT : X3AC	
Quanta Computer Inc.	
Size	Document Number: MEMORY_C_LPDDR4 Rev: 3A
Date: Wednesday, October 07, 2020	Sheet 19 of 57

Non-NB Footprint:bga200-hynix-h9hcnnnbkmalhr-0_5s

LPDDR4 CH-D



PROJECT : X3AC
Quanta Computer Inc.
Size
Document Number
MEMORY_D_LPDDR4
Rev
3A
Date: Wednesday, October 07, 2020
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+3V 8,11,13,14,15,37,43,46,47,50,52,53,54,55,57,58,59,78,87,89
+VIN 37,78,80,82,83,84,87,88,92
+3V_CS 53,89

LID Switch

0210 reserve control by EC

8 EC_BLON
R3402 @ *1K_1%_2

8,47 EMU_LID
R3405 @ *Short_0201
PN_BLON
D3400
MEK500V-40T1G
BLON_CON
R3403 100K_1%_2
C3411 22P/25V_2

4,6,34 PCH_LVDS_BLON
PCH_LVDS_BLON
R3404 1K_1%_2
R3406 100K_1%_2

For privacy panel schematic

+3VS5
+3V
R3438 @ *Short_0402
R3439 @ *0_5%_4

8.1 Function table

Table 5: Function table (1)

Input S	Channel on
L	B0
H	B1

(1) H = HIGH voltage level; L = LOW voltage level.

when PRIVACY panel,LCD_PRIVACY_R is high

EDP@ U3402
74LVC1G3157GW
47 PWM_EC_OUT
PWM_EC_OUT
4,47 PCH_DPST_PWM
PCH_DPST_PWM
LCD_PRIVACY_R
VADJ1_R
EDP@ R3427 1K_1%_2
VADJ1
EDP@ C3404 33P/25V_2
EDP@ R3401 100K_1%_2
R3400 @ *0_5%_2
R3426 @ *0_5%_2

01/15 For privacy panel U3402 & R4744 Stuff,R3400 non-Stuff
If EC Code ready,Switch can cost down,R3400 & R3426 Stuff, U3402 non-stuff

CPU 11 LCD_PRIVACY_PCH
R3417 @ *Short_0402
LCD_PRIVACY_R
R3419 100K_1%_2

R3416 Poly Fuse

for TS power

+3V
+3V_TS
Width >= 20mil
@ C3417 *1uF/6.3_2
@ U3400 *G5245AT11U
IN#2 IN#1 EN OUT GND
OLED@ C3419 *0.1U/10V_2
@ C3420 *1U/6.3V_4
4,6,34 PCH_LVDS_BLON
R3422 @ *10K_5%_4
13,34 TS_RST#
R3420 @ *10K_5%_4

+VIN
+VIN_BLIGHT
EDP@ Q3403 AO3409
EDP@ R3434 100K_1%_4
EDP@ C3426 0.1u/25V_4
EDP@ R3433 10K_5%_2
PCH_LVDS_BLON#
4,6,34 PCH_LVDS_BLON
EDP@ Q3404 2N7002KW
@ R3432 *100K_5%_2

High=Backlight PWR Turn ON
LOW=Backlight PWR Turn OFF

For S5/MSC Turn off the Backlight

+3V
@ R3421 *1K_1%_2
@ C3418 1u/10V_2
4,92 PCH_DISP_ON
U3401 G517AH1RB1U
IN OUT FLAG/EN DSG GND EPAD SET
LCD_P
R3423 220_1%_2
LSET R3424 7.68K_1%_4
RSET
R3425 100K_1%_2
L3402 MHC1608P260Z06BP6A0
+3VLCD_CON
RF requirement 02/22
C3421 0.01U/10V_2
C3422 0.1U/10V_2
C3423 10U/6.3V_4
@ C3425 *68p/25V_2
C3424 100p/25V_2

Width >= 80mil

G517AH	
RSET(KΩ)	Current Limit(A)
7.68	2.7
10.5	2
21	1
42	0.5

+3V
L3400 @ *Short_0402
+3V_TS
+3V_HOME
L3401 @ *0_5%_4
Width >= 20mil

4 DDIA_TXP_3	C3400	0.1U/10V_2	INT_EDP_TXP3_C
4 DDIA_TXN_3	C3401	0.1U/10V_2	INT_EDP_TXN3_C
4 DDIA_TXP_2	C3402	0.1U/10V_2	INT_EDP_TXP2_C
4 DDIA_TXN_2	C3403	0.1U/10V_2	INT_EDP_TXN2_C
4 DDIA_TXP_1	C3405	0.1U/10V_2	INT_EDP_TXP1_C
4 DDIA_TXN_1	C3406	0.1U/10V_2	INT_EDP_TXN1_C
4 DDIA_TXP_0	C3407	0.1U/10V_2	INT_EDP_TXP0_C
4 DDIA_TXN_0	C3408	0.1U/10V_2	INT_EDP_TXN0_C
4 DDIA_AUX_P	C3409	0.1U/10V_2	INT_EDP_AUXP_C
4 DDIA_AUX_N	C3410	0.1U/10V_2	INT_EDP_AUXN_C

+3V_HOME Power for Accelerometer +e-Compass+Gyro use.

+3V_TS
13 TS_INT#
TS_INT#_CN
Q3402 DMG1012T-7
R3410 *20K_1%_2
13,34 TS_RST#
R3411 @ *0_5%_2
TS_RST#_CN
OLED@ C3412 *0.1U/10V_2
47 TS_RST_EC#
R3435 @ *Short_0402

+3V
8 ISH_GYRO_INT
ISH_GYRO_INT
@ Q3401 *DMG1012T-7
GYRO_INT
R3409 0_5%_2
To PCH
To GYRO

Nomal Touch Screen
D3401 MESD0521PSCR1
D3402 MESD0521PSCR1
8 I2C0_SDA_TS
8 I2C0_SCL_TS
R3414 @ *Short_0402
R3415 @ *Short_0402
I2C0_SDA_TS_R
I2C0_SCL_TS_R

+3V_TS
@ R3436 *20K_1%_2
TS_OFF#
@ R3437 *100K_1%_2

eDP Conn.

WWAN sku FP: lvds-50406-04071-001-40p-r
WLAN sku FP: 51693-0400t-v01-40p-l

DFHS40FR243
CN3400 50473-0400S-V01

4 CPU_EDP_HPD
R3408 1K_1%_2
CPU_EDP_HPD_R
VADJ1
LCD_PRIVACY_R
BLON_CON
+3VLCD_CON
+3V_TS
+3V_HOME
13,47 TS_OFF#
TS_OFF#
I2C0_SCL_TS_R
I2C0_SDA_TS_R
TS_INT#_CN
TS_RST#_CN
SMCLK4
SMDAT4
GYRO_INT
ROM_SCL
ROM_SDA
OLED_EN
+LCD_BLIGHT
Width >= 80mil

Touch Screen
GYRO/E-Compass
Dream Color

53 SMCLK4
53 SMDAT4
54 SMCLK_AC2
54 SMDAT_AC2
R3430 @ *Short_0201
R3431 @ *Short_0201

INT_EDP_AUXN_C
INT_EDP_AUXP_C
INT_EDP_TXN1_C
INT_EDP_TXP1_C
INT_EDP_TXN0_C
INT_EDP_TXP0_C
INT_EDP_TXN2_C
INT_EDP_TXP2_C
INT_EDP_TXN3_C
INT_EDP_TXP3_C

eDP/OLED BOM option item

92 OLED_EN_R
OLED_EN_R
R3428 @ *Short_0201
OLED_EN

+VIN_BLIGHT
+LCD_BLIGHT
F3400 EDP@ LP-MSM150/24/1.5A/24V_4532
+VLVDD
+OLEDVDD
F3401 OLED@ *0_5%_8
f2_1x1_35-2_2-0_75h
+VLVSS
+OLEDVSS
F3402 OLED@ *0_5%_8
f2_1x1_35-2_2-0_75h
OLED@ CN3401 *50376-00601-V01
DFHD06MR075
For normal F3400 Stuff, F3401 F3402 non-Stuff
For OLED F3400 un-Stuff, F3401 F3402 Stuff

OLED Panel Vin Cap

+OLEDVDD
OLED@ C3427 *2.2u/25V_4
OLED@ C3428 *0.1U/25V_4
+OLEDVSS
OLED@ C3429 *2.2u/25V_4
OLED@ C3430 *0.1U/25V_4

Panel Vin Cap

+LCD_BLIGHT
C3413 4.7U/25V_6
C3414 2.2u/25V_4
C3415 0.1U/25V_4
C3416 0.1U/25V_4

Poly Fuse

Vender	Size	P/N
WYN	0805	DK150TPU025 (LP-ISML150)
LFI	0805	DK150TPU022 (0805L150ULYR)
PYS	0805	DK150TPU018 (SPR-P150)

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Quanta Computer Inc.
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SDW Only

01/24 Delete HDA Co-lay

+5V_AVDD >40mils trace

+5V_AVDD → L3601 HCB1005KF-181T15_4 → +5V

+5V_AVDD: C3603 0.1U/10V_2, C3604 10U/6.3V_4, C3605 10U/6.3V_4 — close Pin.43 — AGND

+5V: C3606 ULE10201V05A0

+5V_AVDD: ES2@ R3626 10K_5%_2 → AUDIO_CC1; @ R3628 *10K_5%_2 → AGND

AUDIO_CC2: ES2@ R3627 10K_5%_2; @ R3629 *10K_5%_2 → AGND

+1.8V_AVDD → L3600 HCB1005KF-181T15_4 → +1.8V

+1.8V_AVDD: C3600 10U/6.3V_4, C3601 0.1U/10V_2 — close Pin.17 — AGND

+1.8V: C3602 10U/6.3V_4

+1.8V_DVDD → L3602 HCB1005KF-181T15_4

+1.8V_DVDD: C3607 1uF/6.3_2, C3608 0.1U/10V_2, C3609 10u/6.3V_4 — close Pin.5

U3600

+5V_AVDD → AVDD1 (43); +1.8V_AVDD → AVDD2 (17); +1.8V_DVDD → DVDD (5); NC#1 (40), NC#2 (41); AUDIO_CC1 → CC1/NC (1); AUDIO_CC2 → CC2/NC (2)

15 SNDW1_DAT_R → R3600 0_5%_2 → SNDW1_DAT_ADO → 8 SdW_Data

15 SNDW1_CLK_R → R3601 0_5%_2 → SNDW1_CLK_ADO → 9 SdW_CLK

@ C3613 *22p/25V_2, @ C3610 *22p/25V_2, @ C3611 *22p/25V_2, @ C3612 *22p/25V_2

MHDA_RST#_OUT → 10 LSB_MHDA_RST#_0

MHDA_BCLK → 11 MHDA_BCLK

ACZ_SYNC_AUDIO → 12 MSB_MHDA_SYNC

13 MHDA_SDATA-IN

14 MHDA_SDATA-OUT

ALC711_GPIO_2 → 15 NC/GPIO_2/DMICDATA2

RTCLK_32K → R3634 @ *0_5%_4 → ES2@ R3630 0_5%_4 → SUSCLK_AUDIO_32K → 3 RTCLK_32NC

14,41 SUSCLK_32K

C3615 @ *10P/50V_2 → HD_SDW_SEL → 4 HD_SdW_SEL

37,46 DIGITAL_D1 → R3605 @ *0_5%_2 → DMIC0 → 6 DMIC_DATA

46 DIGITAL_CLK → R3606 @ *0_5%_2 → DMIC_CLK_R → 7 DMIC_CLK

C3616 @ *10P/50V_2

50 MUTE_LED_CNTL → R3652 0_5%_2 → MUTE_LED_CNTL_R → 47 LINE2/JD2

JD1 → 48 AGPI/HP/LINE1/JD1

CBN_24 → 24 CBN

C3617 ES2@ 2.2U/10V_4 → CBP_21 → 21 NC/CBP

CBP_23_C → C3618 2.2U/10V_4 → CBP_23 → 23 CBP/CBP2

R3613 ES2@ 0_5%_2 → CBN_22 → 22 NC/CBN2

HP-OUT-R/USB-DP_OUT → 26 → HPOUT_R → HPOUT_R 76

HP-OUT-L/USB-DN_OUT → 27 → HPOUT_L → HPOUT_L 76

RING2/MIC2-L/MIC2-VREFO-L → 30 → MIC2_VREFO_L_30

MIC2_CAP/RING2/MIC2-L → 32 → R3602 ES2@ 0_5%_2 → AGND

SLEEVE/MIC2-R/MIC2-VREFO-R → 31

5VSTB/SLEEVE/MIC2-R → 33 → MIC2_R_C_33 → R3604 ES2@ 0_5%_4 → EXT_MIC_L_C

LINE1-R → 35

LINE1-L → 36

LINE2-L → 44

LINE2-R → 45

MIC2-VREFO-L/USB-DP-IN → 28

MIC2-VREFO-R/USB-DN-IN → 29

LINE2-VREFO/NC → 46

ALC3304-CG

AL003304001

LDO2_CAP → 18; AVSS1 → 37; AVSS2 → 19; NC/CPVEE/CPVPP → 20; CPVEE/CPVPP → 25; LDO4_NC → 42; LDO1_CAP → 39; NC/MIC2_CAP → 34; LDO3_CAP → 16; VREF → 38; EPAD → 49

LDO2_CAP_18 → AGND

CPVEE_20

CPVPP_25

CODEC_VREF

LDO4_CAP

LDO1_CAP

LDO3_CAP

LDO2_CAP_34

C3619 10U/6.3V_4 — AGND

ES2@ C3620 2.2U/10V_4 — AGND

C3621 2.2U/10V_4 — AGND

ES2@ C3622 10U/6.3V_4 — AGND

R3616 100K_1%_2 — C3623 10U/6.3V_4 — AGND

ES2@ C3624 10U/6.3V_4 — AGND

C3625 10U/6.3V_4 — AGND

C3626 2.2U/10V_4 — C3627 0.1U/10V_2 — close Pin.38 — AGND

SDW Slave mode Stuff

R3608 3K_1%_4 → MHDA_BCLK

R3611 100K_1%_2 → HD_SDW_SEL

when DIGITAL MIC to CODEC, SPK_ID_CODEC is SPK ID
when DIGITAL MIC to PCH, DMIC0 is SPK ID

+1.8V_DVDD: @ R3632 *1K_5% → Y3600 VDD, OUT → RTCLK_32K; OE, GND; @ R3633 *0_5%_2 → GND

Y3600 *32.768K/10ppm

MIC2_VREFO_L_30 → R3609 ES2@ 2.2K_5%_4 → EXT_MIC_L_C → EXT_MIC_L_C 76

+5V: R3631 @ *10K_5%_2 → JD1

+1.8V_DVDD: ES2@ R3614 10K_1%_2; ES2@ R3615 0_5%_2 → SENSE_A → SENSE_A 76

Need double check AMP sequence

+1.8V_DVDD: R3619 10K_1%_2 → AMP_PD#

47 VOLMUTE# → D3600 MEK500V-40T1G → AMP_PD# → AMP_PD# 37

@ R3620 *100K_1%_2, @ C3630 *0.1U/16V_4

MHDA_RST#_OUT → R3623 @ *0_5%_2

15 ACZ_RST#_AUDIO → R3624 @ *0_5%_2

Q3600 *MMBT3904T-7-F-01

R3622 *100K_1%_2 → +1.8V_DVDD

MHDA_RST#_OUT is output pin only,
Please don't connect to PCH audio controller.

C3628 @ *0.1U/10V_4

C3629 @ *1000p/50V_4

AGND

R3621 @ *0_8/S

AGND

<R3621> Place at Codec bottom side.
<C3628 & C3629> Place near audio connector. Don't short this pad to USB digital ground, and should be far away from any power traces.

ALC711_GPIO_2 → R3651 0_5%_2 → PRIV_MIC_LED# → PRIV_MIC_LED# 50

01/15 for microphone mute LED control

SdW Pad Driving control

DMIC_DATA and GPIO_2 support power on strap driving control only for ES-2

+1.8V_DVDD

DMIC0 → R3647 @ *10K_5%_2; R3648 @ *10K_5%_2

ALC711_GPIO_2 → R3641 @ *10K_5%_2; R3642 @ *10K_5%_2

DMIC_CLK_R → R3649 @ *10K_5%_2; R3650 @ *10K_5%_2

For ES-1 and ES-2, DMIC_CLK support power on strap driving control

ACZ_SYNC_AUDIO → R3643 @ *10K_5%_2; R3644 @ *10K_5%_2

MHDA_RST#_OUT → R3645 @ *10K_5%_2; R3646 @ *10K_5%_2

for ES-2 SdW slave ID power on strap only, please reserved if needed.

PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio ALC3292-CG	3A

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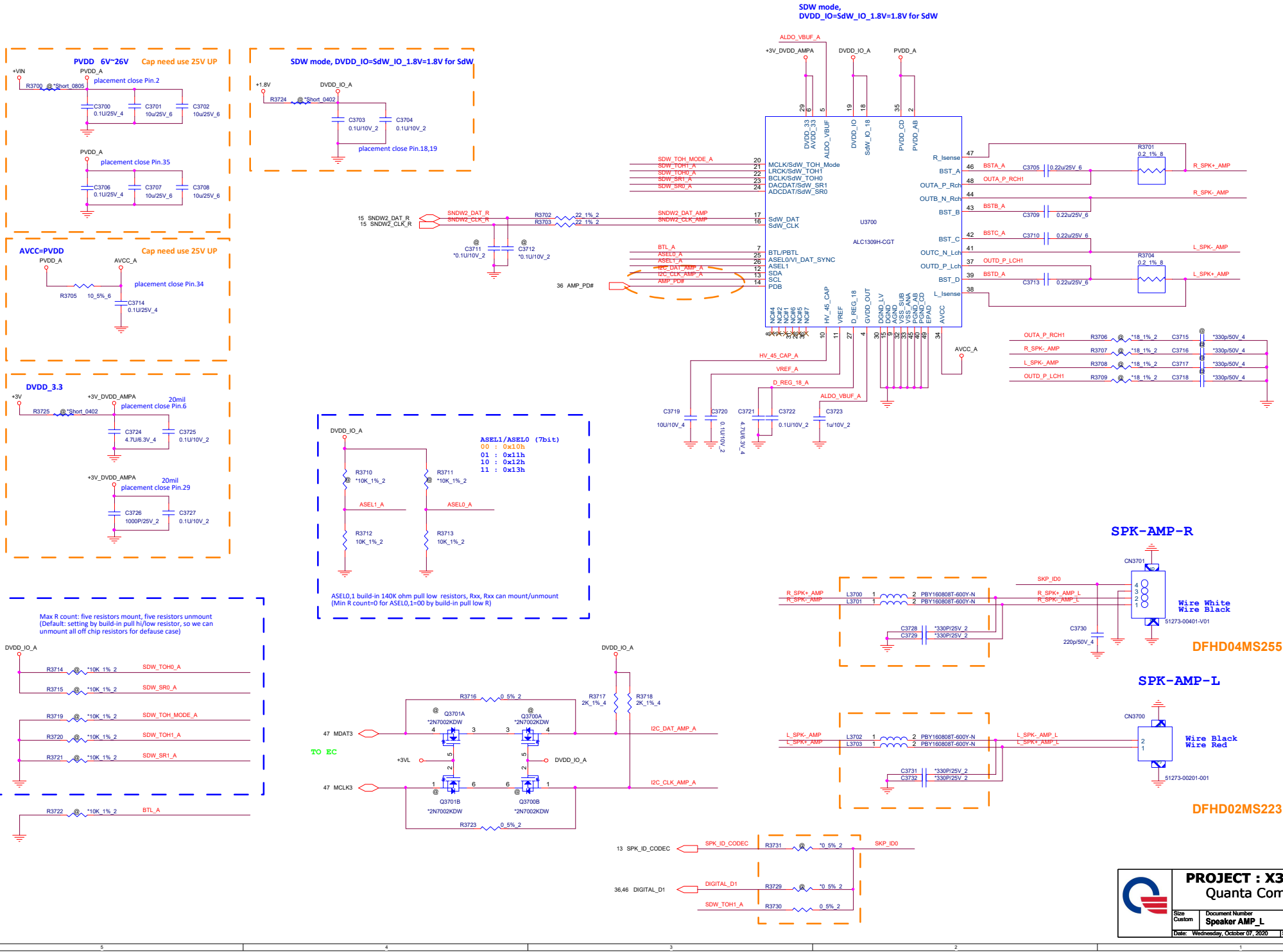
Speaker AMP



PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Speaker AMP_L	3A

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WLAN/BT Harrison Peak SD-1216 ADPCAX20042

If CNVi is present CNVi = Low, low switch will never turn off
If CNVi is not present CNVi = High, load switch EN pin will follow WLAN_DISABLE

Windstorm Peak & Jefferson Peak 2 M.2 1216 co-layout
Intel Dual Band Wireless-AC 8265
Intel Dual Band Wireless-AC 9560

WLAN co-lay PCIE cancel

WLAN co-lay PCIE cancel

RF

Support Wake Function(Reserve)

Dual MOS Q4102 must be STUFF

100mil

100mil

Follow CNVi Only Checklist Delete PE_WAKE#

01/15 change power rail

CPU/BATT/FAN NUT MBX3A002010

2D BARCODE

HOLE

GND GUARD clip pad

DDR

SSD

SSD NUT WWAN NUT M6Y0F004010

PROJECT : X3AC	
Quanta Computer Inc.	
Size: Custom	Document Number: WLAN/BT/HOLE
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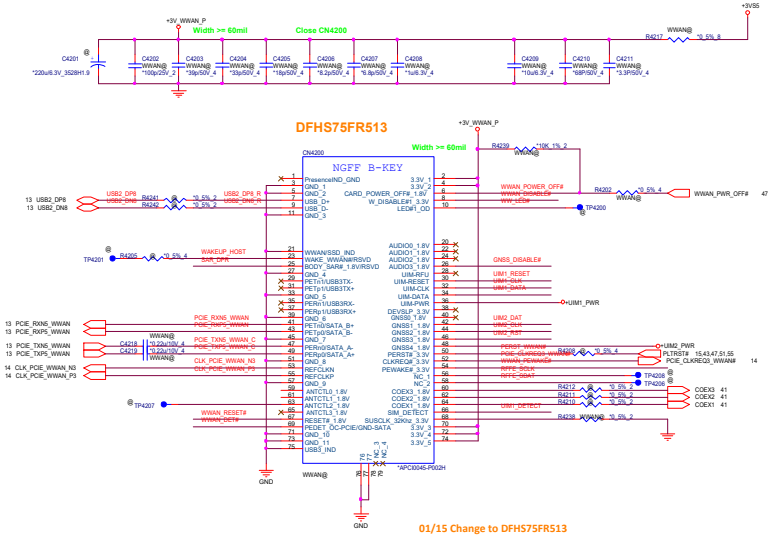
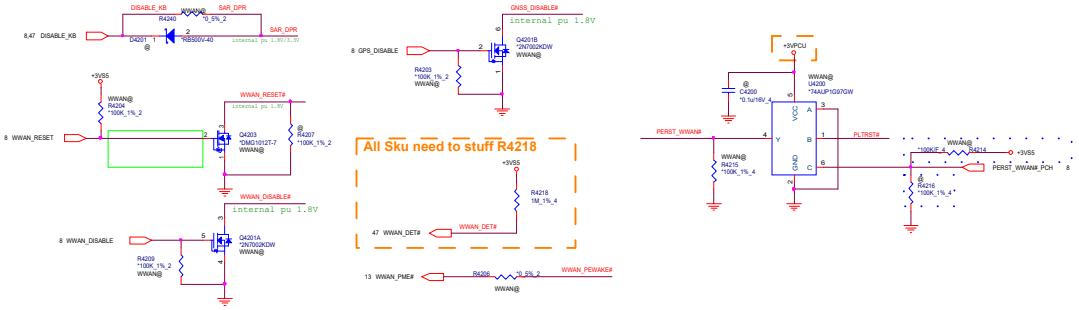
WWAN

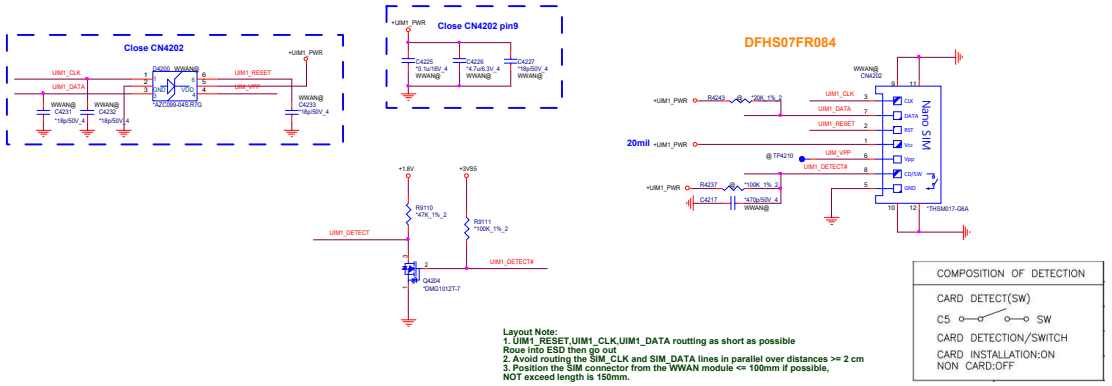
WWAN(Option)
Control of power must be allowed in all S0, S3, S4 and S5 states.



GPIO



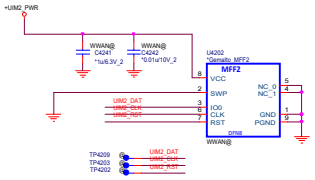
SIM Card



Layout Note:
1. UIM1_RESET,UIM1_CLK,UIM1_DATA routting as short as possible
Roue into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances >= 2 cm
3. Position the SIM connector from the WWAN module <= 100mm if possible,
NOT exceed length is 150mm.

MIMO

eSIM



Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

PROJECT : X3AC Quanta Computer Inc.		
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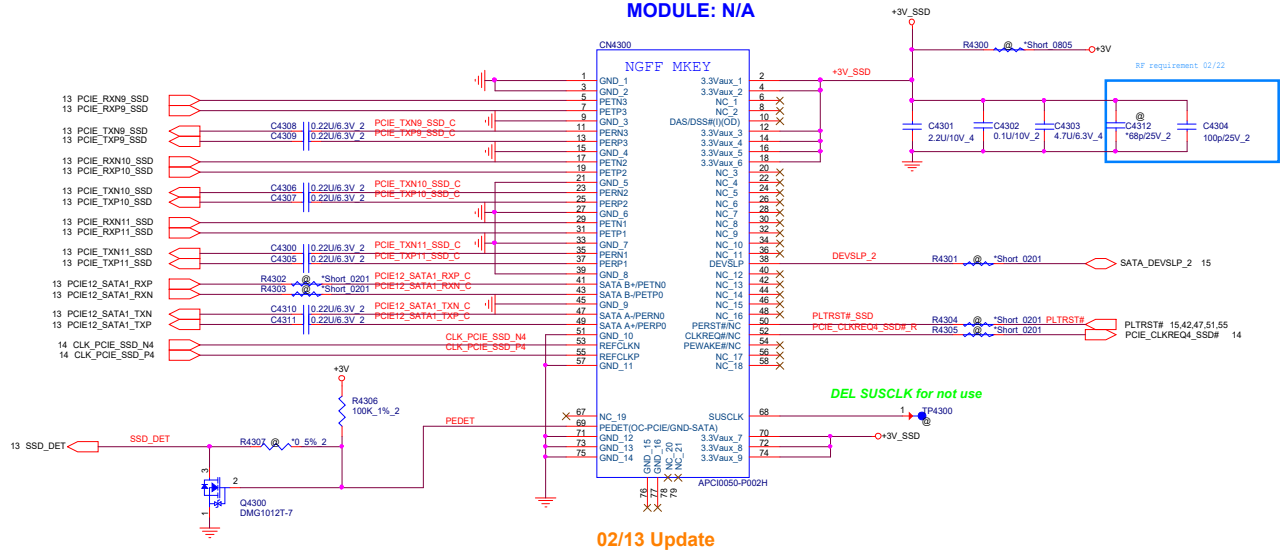
SSD CONN



PROJECT : X3AC		
Quanta Computer Inc.		
Size: Custom	Document Number: SSD	Rev: 3A
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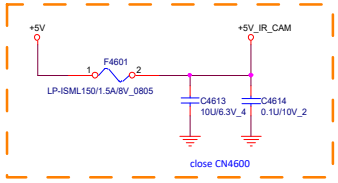
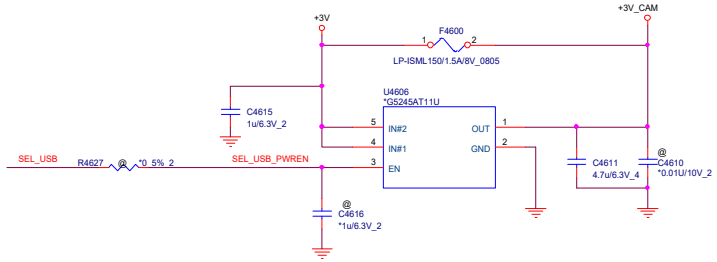
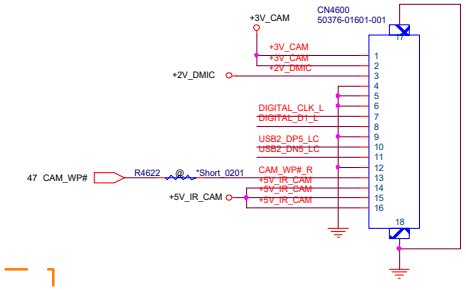
IR CAM PWR



IR CAM PWR For SFH4770S



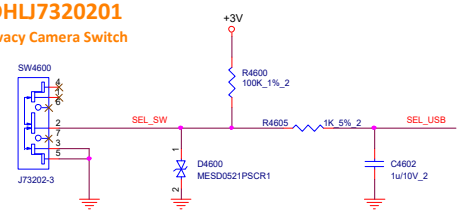
CAMERA CONN



DFHD16MR050
50376-01601-001-16p-l

DHU7320201

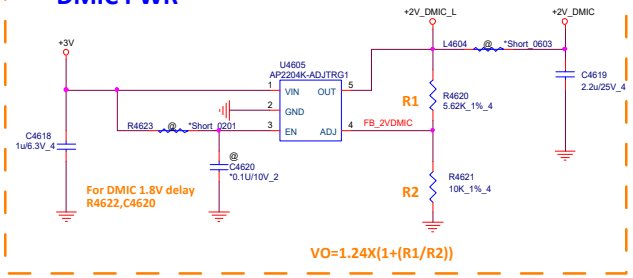
Privacy Camera Switch



High=Camera ON
LOW=Camera OFF

Need Choose Correct Switch

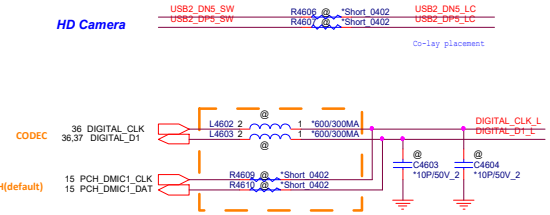
DMIC PWR



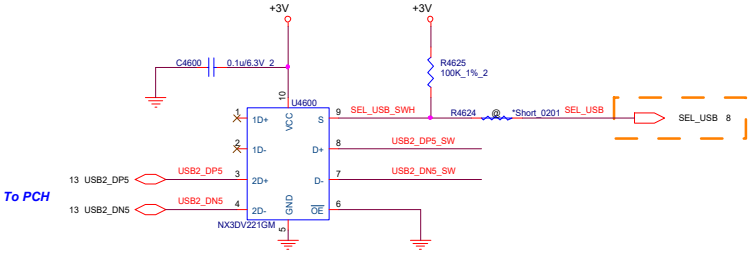
For DMIC 1.8V delay
R4622,C4620

VO=1.24X(1+(R1/R2))

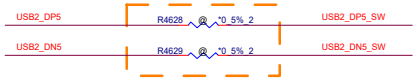
HD Camera



Place together



To PCH



Co-lay with U4600

Poly Fuse

Vender	Size	P/N
WYN	0805	DK150TPU025 (LP-ISML150)
LFI	0805	DK150TPU022 (0805L150ULYR)
PYS	0805	DK150TPU018 (SPR-P150)

8. Functional description

Table 4. Function table[1]

Input		Channel
S	$\overline{OE}$	
L	L	D+ = 1D+; D− = 1D−
H	L	D+ = 2D+; D− = 2D−
X	H	switches off

PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Camera	3A

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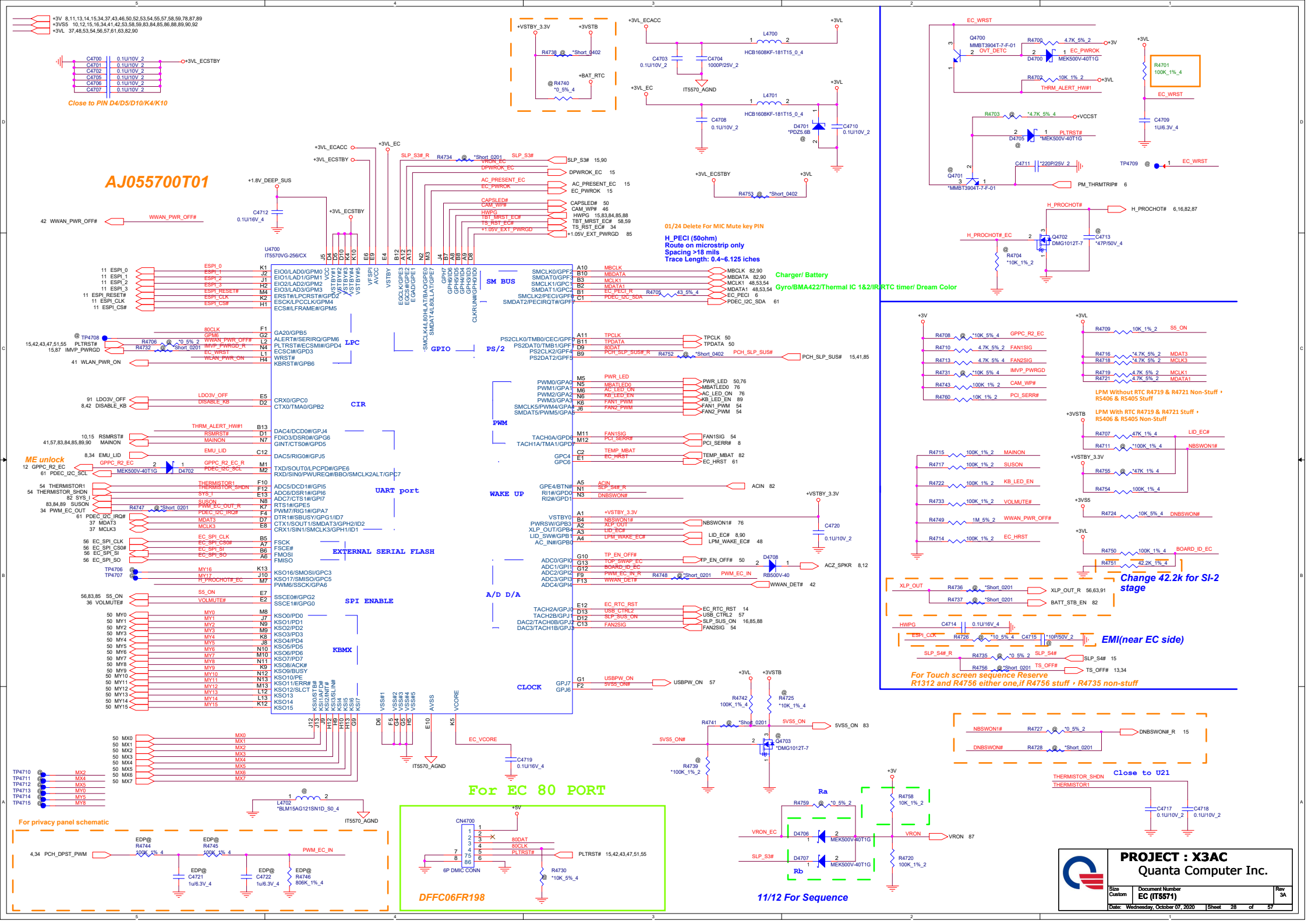
AJ055700T01
U4700
IT5570VG-256/CX
LPC
GPIO
PS/2
SM BUS
CIR
UART port
PWM
WAKE UP
A/D D/A
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
CLOCK
ME unlock
Close to PIN D4/D5/D10/K4/K10
01/24 Delete For MIC Mute key PIN
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
Charger/ Battery
Gyro/BMA422/Thermal IC 1&2/IR/RTC timer/ Dream Color
LPM Without RTC R4719 & R4721 Non-Stuff › RS406 & RS405 Stuff
LPM With RTC R4719 & R4721 Stuff › RS406 & RS405 Non-Stuff
Change 42.2k for SI-2 stage
EMI(near EC side)
For Touch screen sequence Reserve
R1312 and R4756 either one,if R4756 stuff › R4735 non-stuff
Close to U21
For privacy panel schematic
For EC 80 PORT
DFFC06FR198
11/12 For Sequence
PROJECT : X3AC
Quanta Computer Inc.
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EC (IT5571)
Rev 3A
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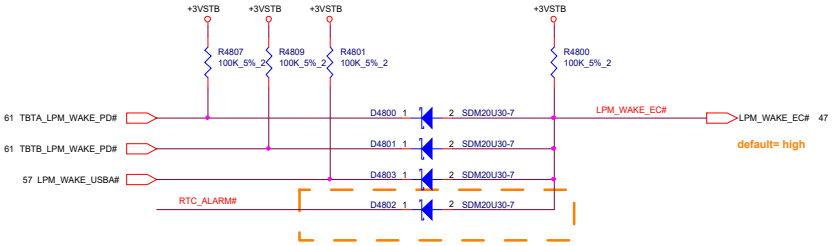
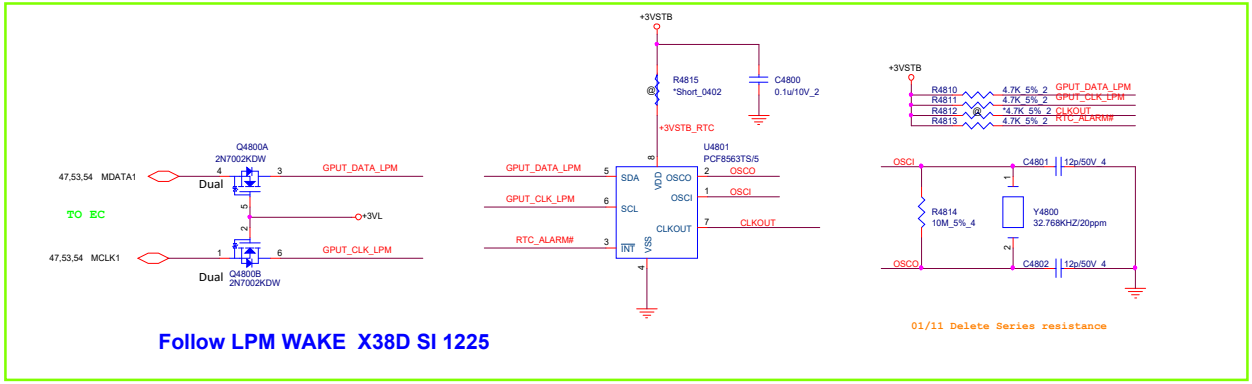


X3A PV For LPM Without RTC Timer Change

EC
BOARD_ID

EC BOARD_ID	ADC	low limit		ADC	high limit	R4750(K ohm)	R4751(K ohm)	P/N
SI	191	0.402580645	ID1		0.728914956	100	20	CS32002FB29
SI-2	207	0.853020528	ID2		1.168093842	100	42.2	CS34222FB00
DB1	223	1.258416422	ID3		1.607272727	100	68.1	
	623	1.663812317	ID4		2.046451613	100	121	
	783	2.114252199	ID5		2.485630499	100	215	
	927	2.564692082	ID6		2.924809384	100	422	



Follow LPM WAKE X38D SI 1225

PROJECT : X3AC
Quanta Computer Inc.

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Custom	EC /NC	3A

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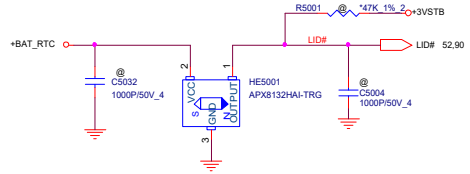
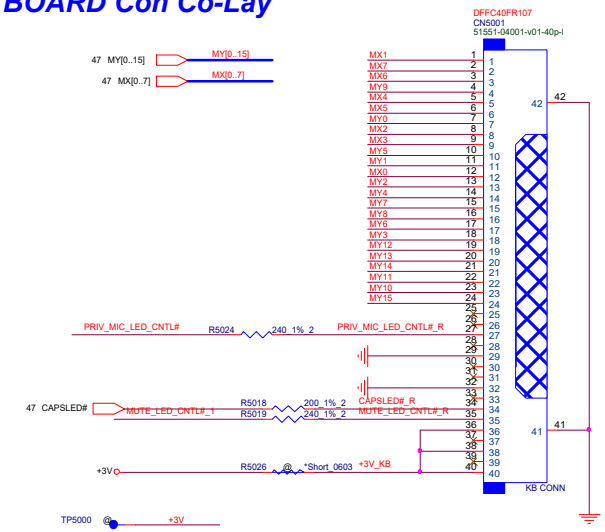
Power Botton Connector and LID



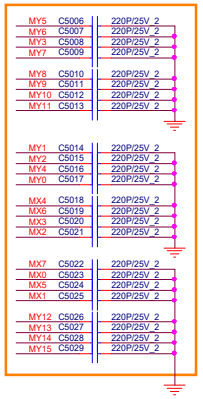
footprint:sot23-2_38-95-3p

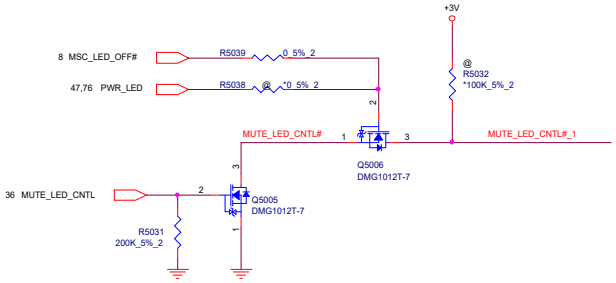
KEYBOARD Con Co-Lay

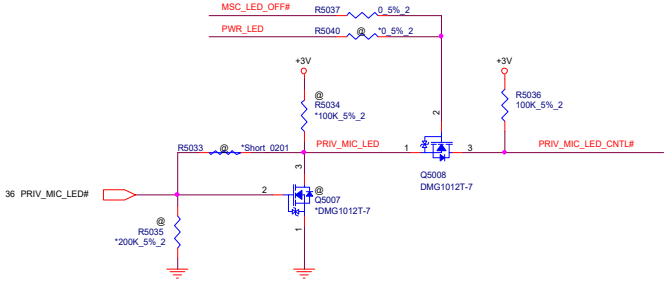
Not Pen Keyboard



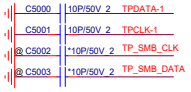
KEYBOARD PULL-UP

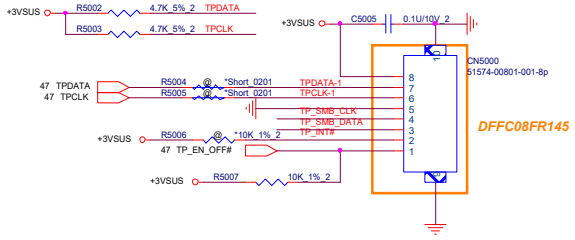


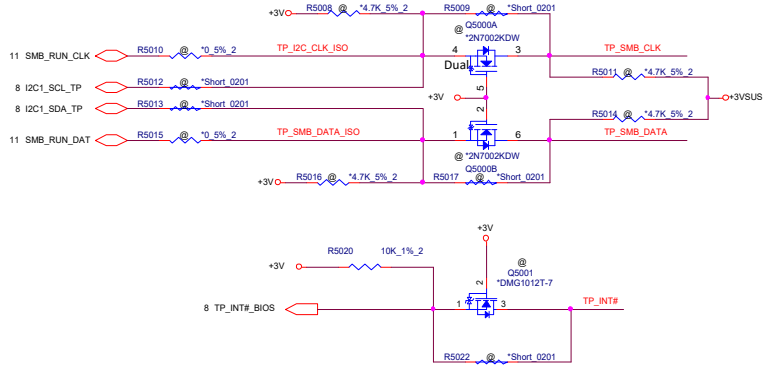




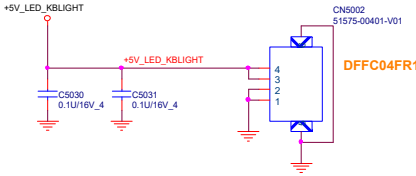
Touch Pad Connector







KB backlight



+3V 8,11,13,14,15,34,37,43,46,47,52,53,54,55,57,58,59,78,87,89
+3VSUS 89
+3VSTB 47,48,56,58,61,63,76,78,82,91
+BAT_RTC 12,14,16,47,82,90,91

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Quanta Computer Inc.		
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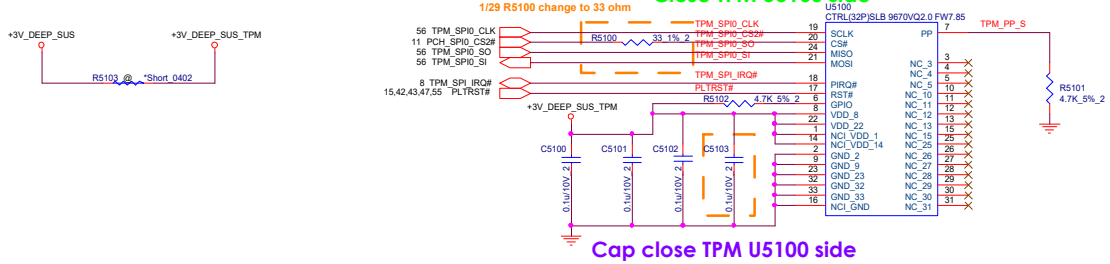
TPM (2.0)

TPM (2.0) SPI SLB 9670VQ2.0 FW7.85

PN:AL009670041

Close TPM U5100 side



Cap close TPM U5100 side

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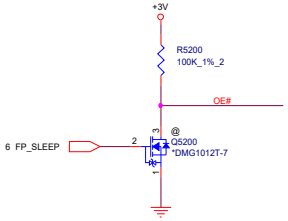
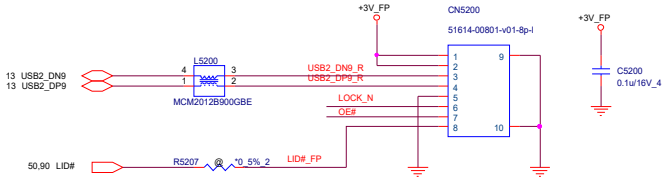
Finger print

8/26 R5208 change to fuse for SVTP 2-55item

FAE not recommand to use SLEEP mode

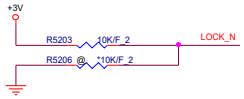


FP CONN



Lock _N for lock ROM data, pull high is no lock and PCH pull low to lock

DFFC08FR126



PROJECT : X3AC Quanta Computer Inc.		
Size: Custom	Document Number: Finger Print	Rev: 3A
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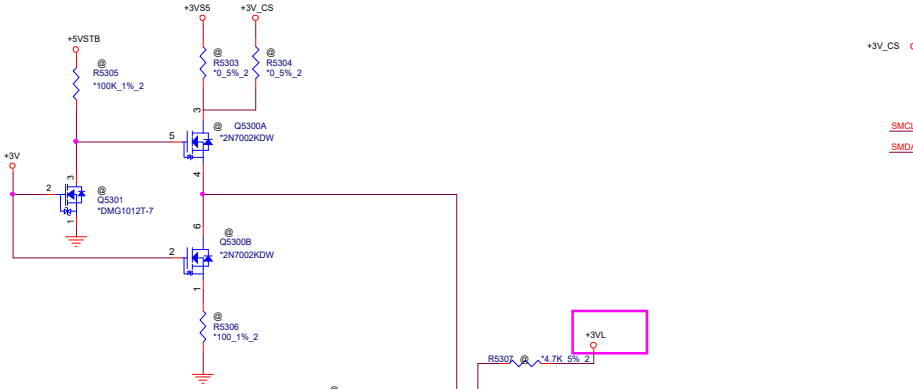
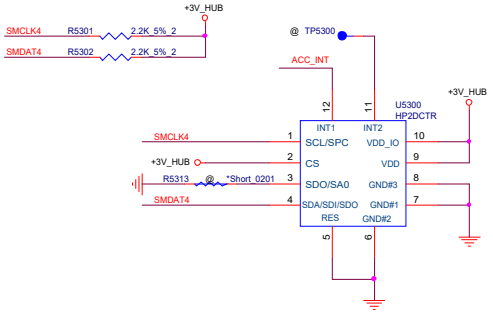
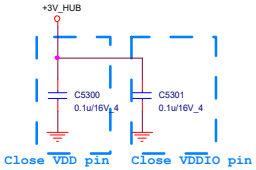
Delete by Ryan

+3V_CS change to power circuit

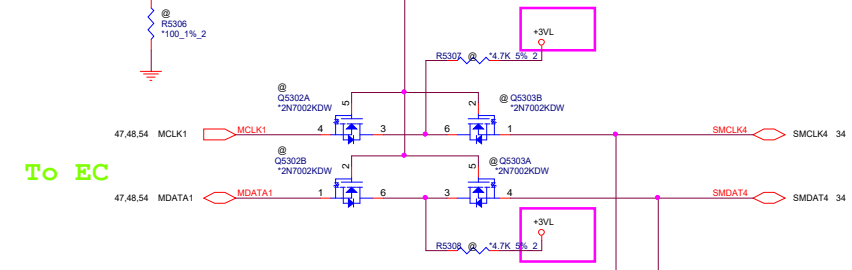
+3V 8,11,13,14,15,34,37,43,46,47,50,52,54,55,57,58,59,78,87,89
+3VS5 10,12,15,16,34,41,42,47,58,59,83,84,85,86,88,89,90,92
+3V_CS 89





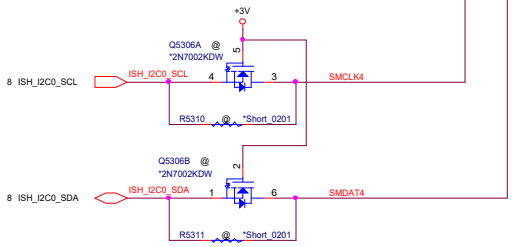


SA0	Address
0	0101000b
1	0101001b

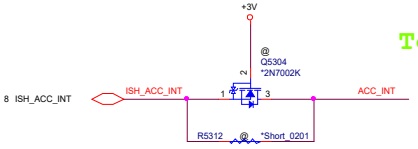


To EC

To GYRO



To PCH



To PCH

To ACC

Quanta Computer Inc.	PROJECT : X3AC		
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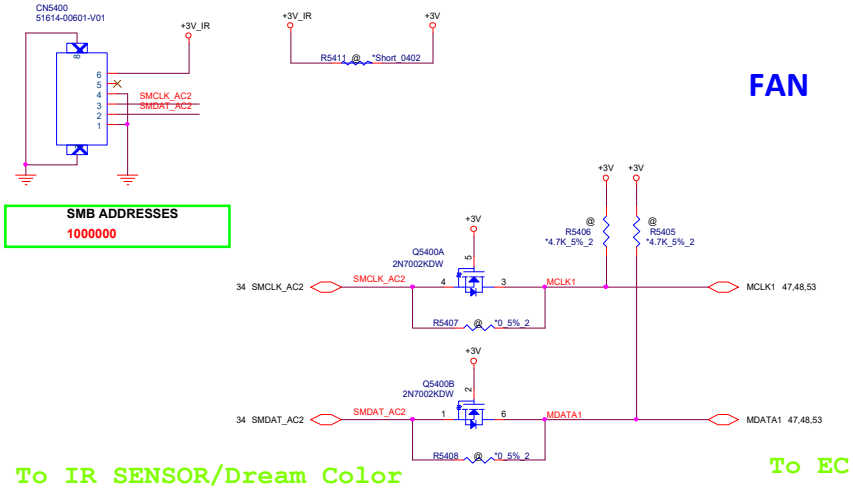
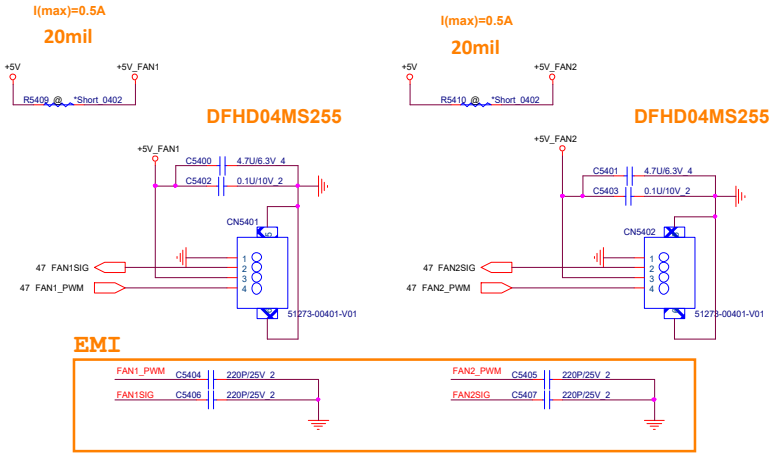
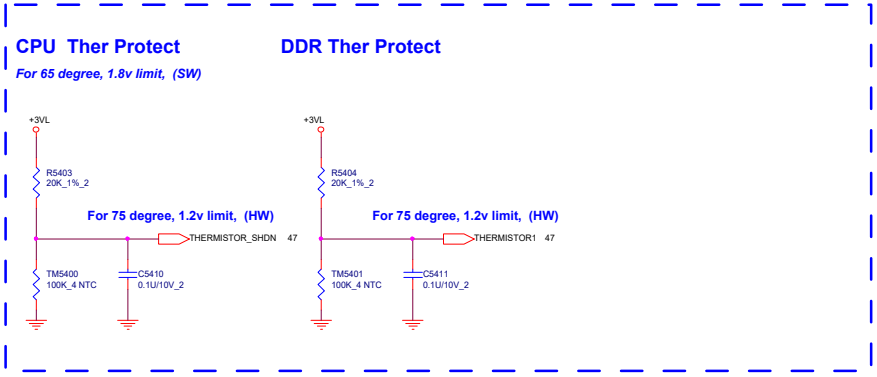
IR connector

DFFC06FR198



FAN





01/17 Delete Thermal Sensor IC

PROJECT : X3AC Quanta Computer Inc.		
Size: Custom	Document Number: FAN / Thermal	Rev: 3A
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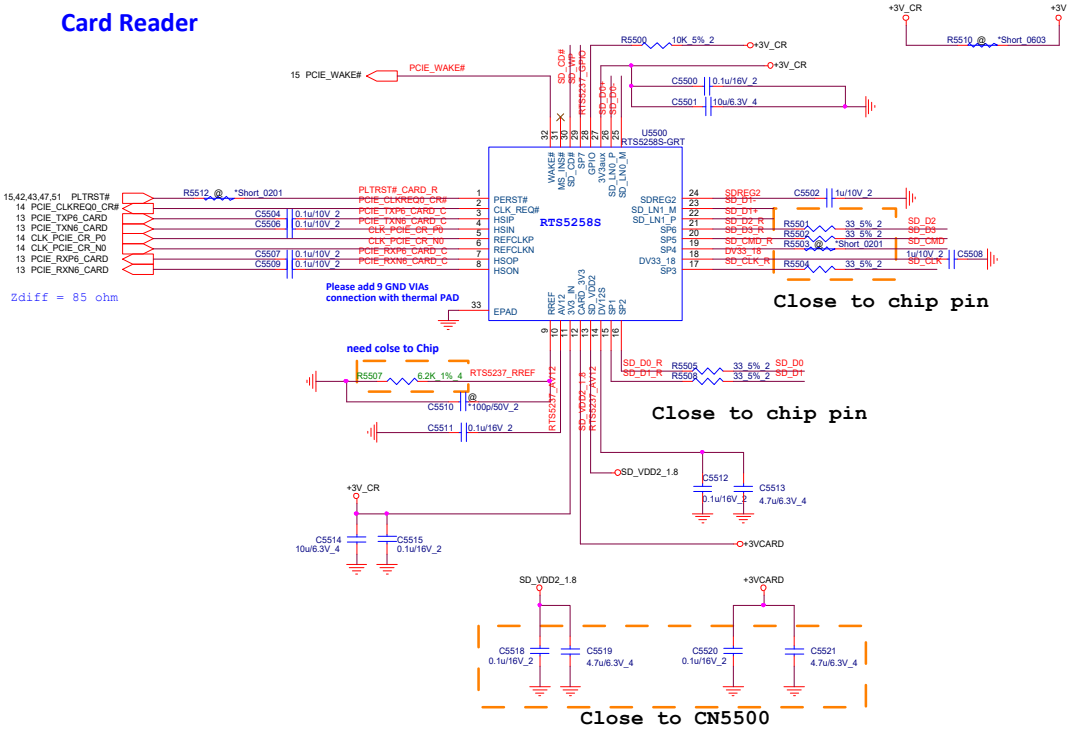
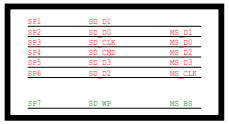
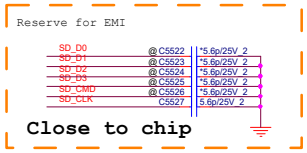
Card Reader





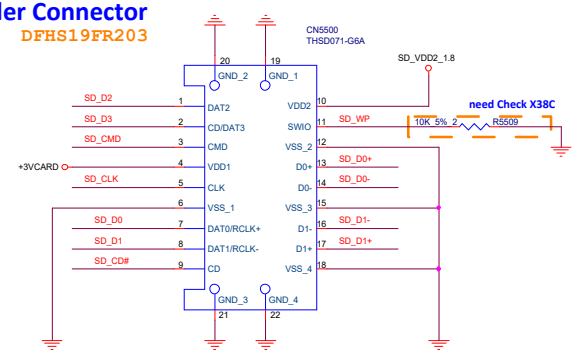
Share Pin

SD / MMC



Card Reader Connector

DFHS19FR203



sdcard-thsd071-g6a-18p

creat support SD4.0 Conn

	PROJECT : X3AC Quanta Computer Inc.	
Size: Custom	Document Number: **Card Reader / RTS5258S**	Rev: 3A
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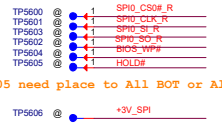
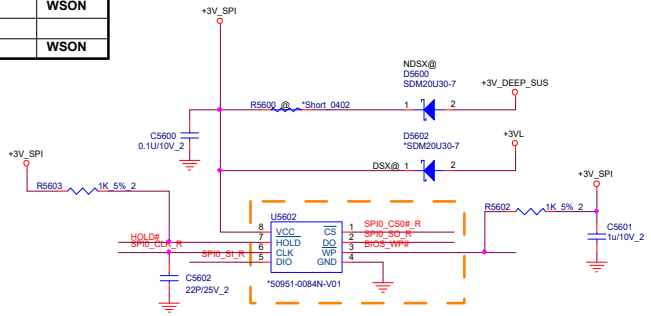
BIOS ROM 16M

PCH SPI ROM(CLG)

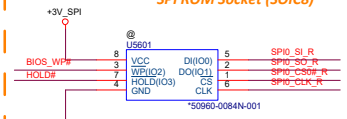
Vender	Size	P/N	Type
MXIC	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)	SOIC
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)	SOIC
GigaDevice	16MB	AKE2DF00Q00 (GD25B127DWIGR)	WSON
Socket		DG008000012 (WSON)	WSON





U5601,U5602,U5603 co-lay

SPI ROM Socket (SOIC8)

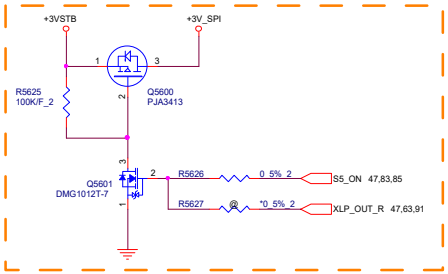


DG008000011

U5601,U5602,U5603 co-lay

Without Boss /SPI ROM Socket (WSON)

DG008000012

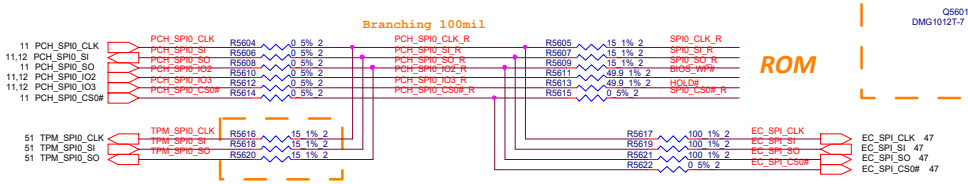


PCH Side

TPM Side

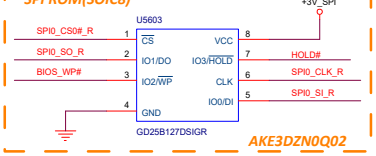
ROM

EC Side



U5601,U5602,U5603 co-lay

SPI ROM(SOIC8)



AKE3DZN0Q02

	PROJECT : X3AC Quanta Computer Inc.		
Size Custom	Document Number Flash ROM (BIOS,EC)		Rev 3A
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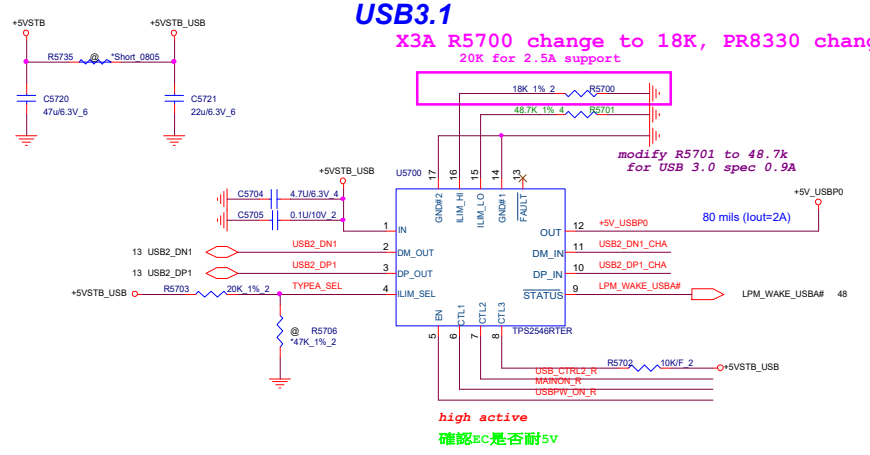
USB3.1

X3A R5700 change to 18K, PR8330 change to 1M

20K for 2.5A support

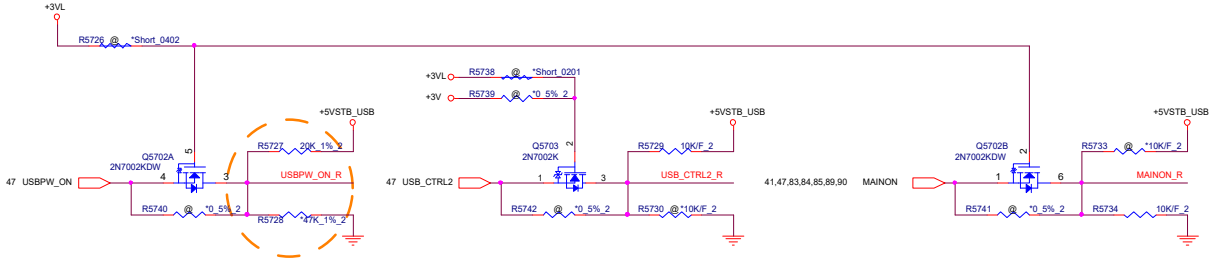


high active

確認EC是否耐5V

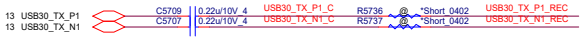
2/11 Delete USB3.1 re-driver

X3A PV For LPM Without RTC Timer Change

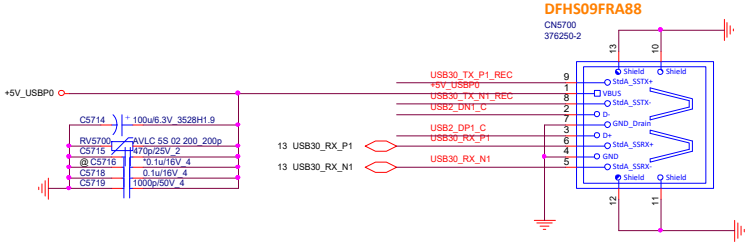


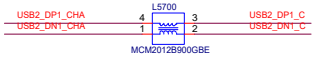
USBPW_ON_R need always ON before EC control

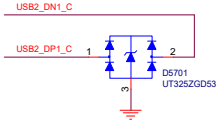
PV BOM Change_0603_J

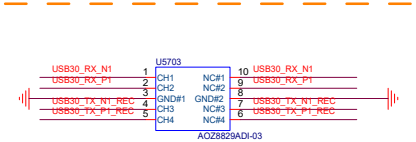


DFHS09FRA88





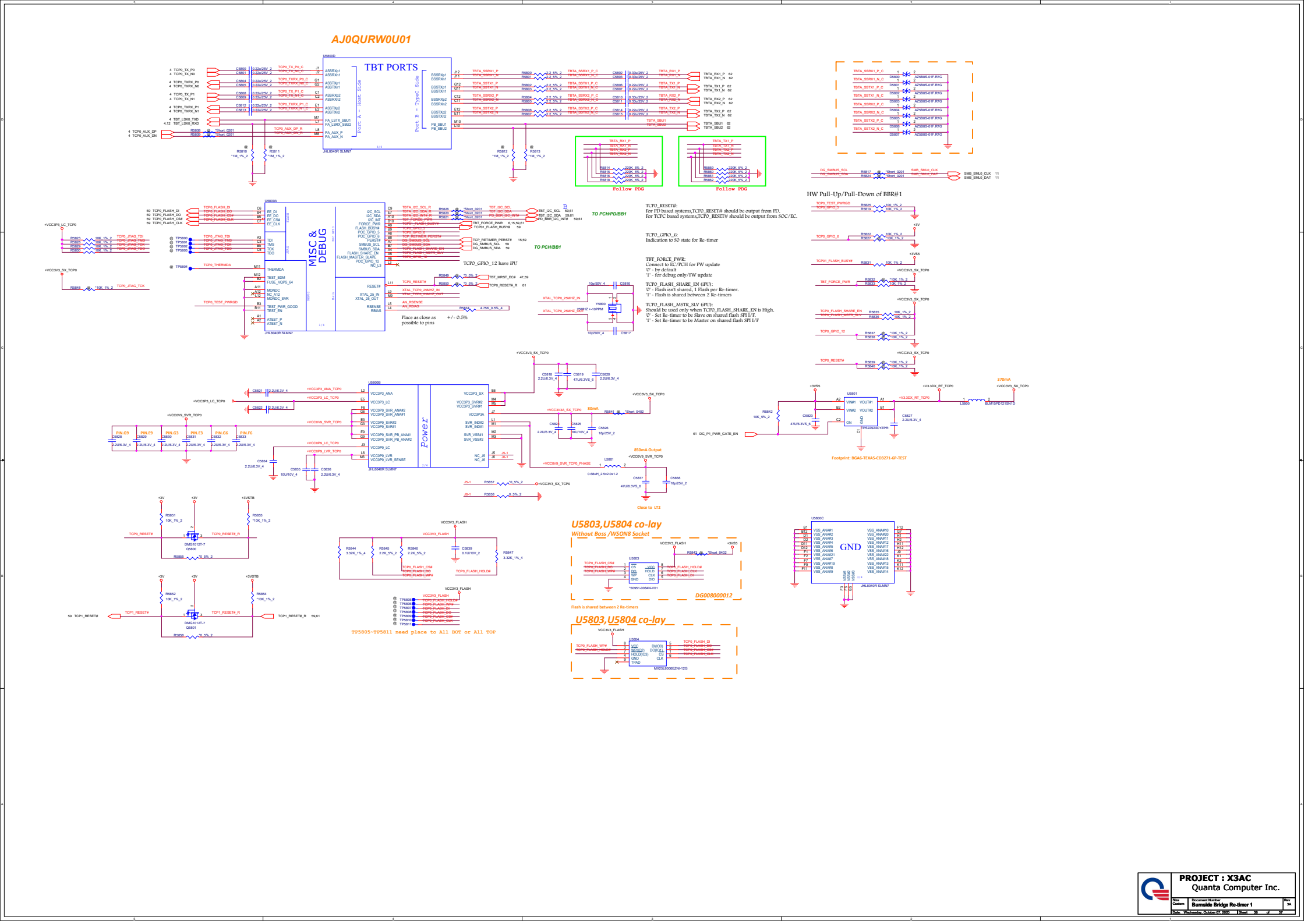




Change to BC008829Z00

Quanta Computer Inc.	PROJECT : X3AC	
Size: Custom	Document Number: USB type A	Rev: 3A
Date: Wednesday, October 07, 2020	Sheet 37 of 57	

AJ0QURW0U01



PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Burnside Bridge Re-timer 1	3A

Date: Wednesday, October 07, 2020 Sheet 36 of 57

AJ0QURW0U01

09/10 SWAP BSSRXP2/N2 for meet RVP

TBT PORTS

Port A - Host Side

Port B - TypeC Side

HW Pull-Up/Pull-Down of BBR#1

Follow PDG

Follow PDG

TCP1_RESET#:
TCP1_RESET# should be output from PD.

TCP1_GPIO_6:
Indication to S0 state for Re-timer

TBT_FORCE_PWR:
Connect to EC/ICH for FW update
'0' - by default
'1' - for debug only/FW update

TCP1_FLASH_SHARE_EN (pU):
'0' - Flash isn't shared, 1 Flash per Re-timer.
'1' - Flash is shared between 2 Re-timers

TCP1_FLASH_MSTR_SLV (pU):
Should be used only when TCP1_FLASH_SHARE_EN is High.
'0' - Set Re-timer to be Slave on shared flash SPI I/F.
'1' - Set Re-timer to be Master on shared flash SPI I/F

TCP1_GPIO_12 have iPU

Place as close as possible to pins

+/- 0.5%

TO PCH/PD/BB0

TO PCH/BB0

80mA

850mA Output

370mA

Close to LT2

Footprint: BGA6-TEXAS-CO3271-6P-TEST

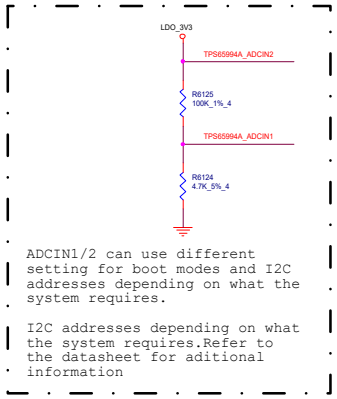
MISC & DEBUG

Power

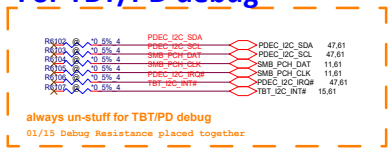
GND

U6101 AL065994T01 TPS65994ADYBGR(DSBGA)

DSBGA (YBG50)-3.2mm x 3.2mm



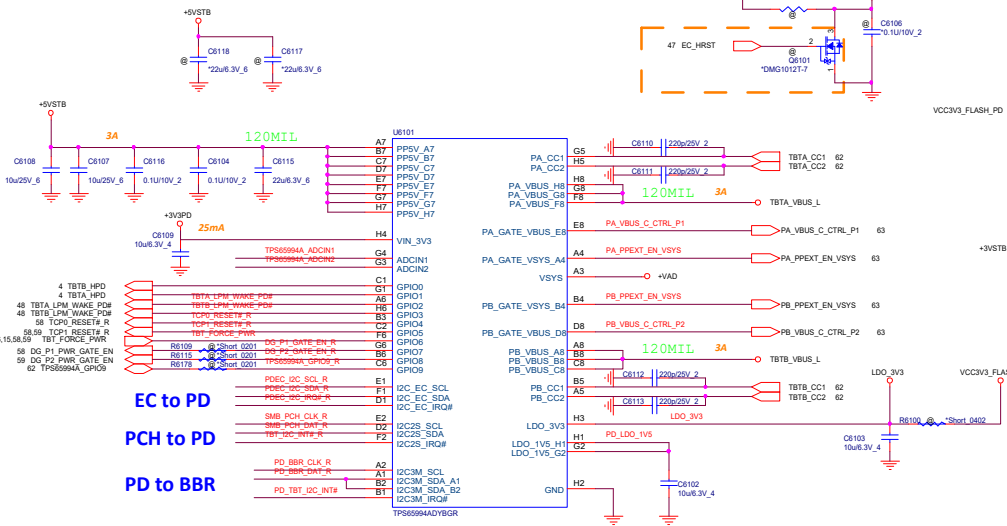
For TBT/PD debug

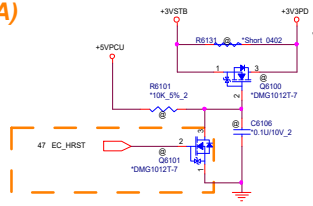


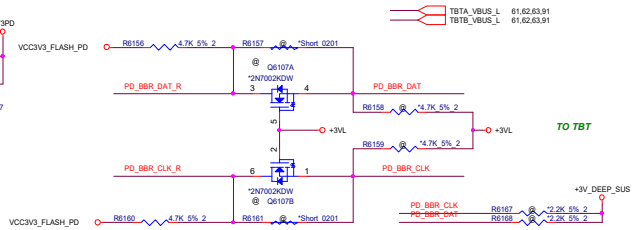
EC to PD

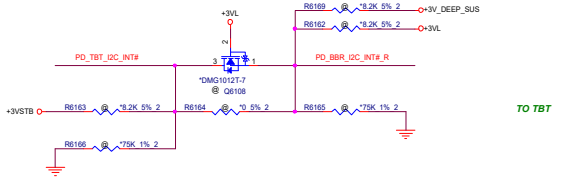
PCH to PD

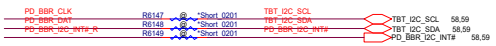
PD to BBR



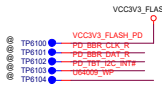








TP6100~TP6103 need place to All BOT or All TOP

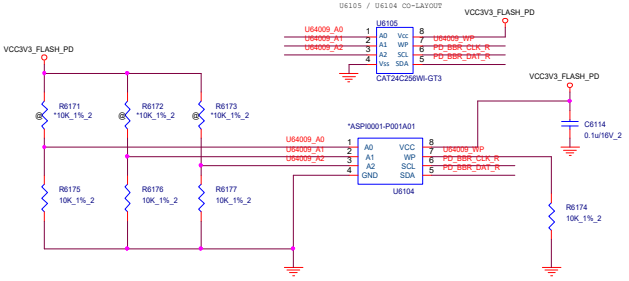


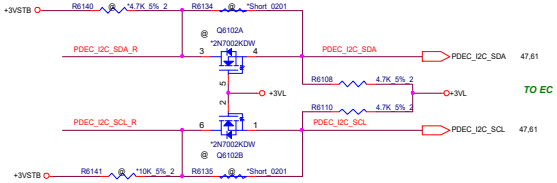
SOIC 8, 150 mils

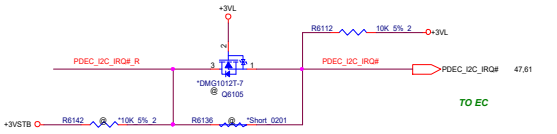
AKE33200R00 / IC EEPROM(8P) CAT24C256WI-GT3(SOIC8)

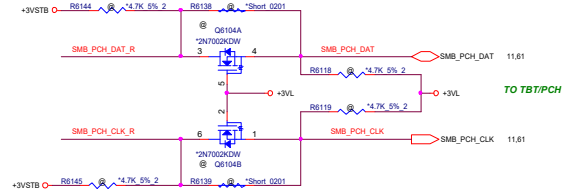
AKE11ZA0A00 / IC EEPROM(8P) AT24C256C-SSHL-T (SOIC)

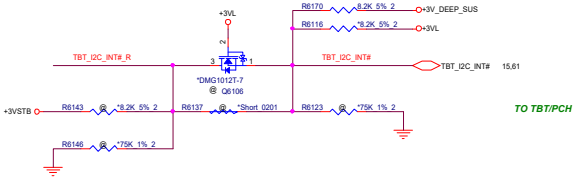
AKE13ZA0P00 / IC EEPROM(8P) BR24G256FJ-3AGTE2(SOP-J8)







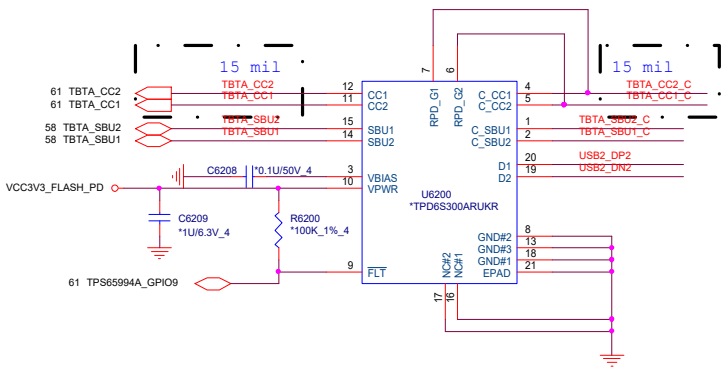




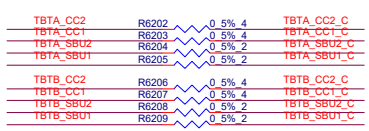
TBTA_VBUS_L 61,62,63,91

TBTB_VBUS_L 61,62,63,91

PROJECT : X3AC Quanta Computer Inc.			
Size Custom	Document Number TPS65994		Rev 3A
Date: Wednesday, October 07, 2020	Sheet 40 of 57		



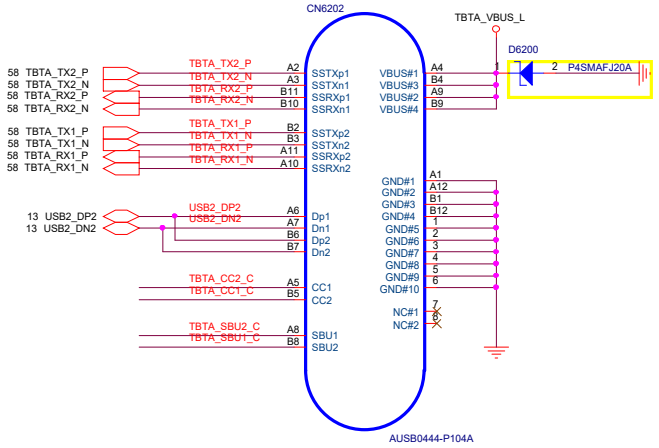
co-layout for ESD option



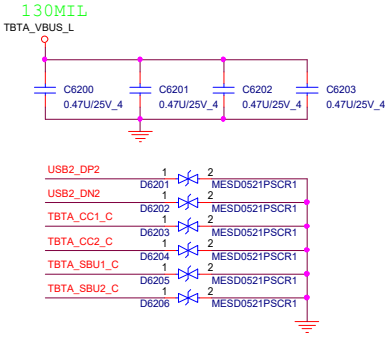
if stuff R6202~R6209 , unstuff U6200,U6201

USB Type-C Port A

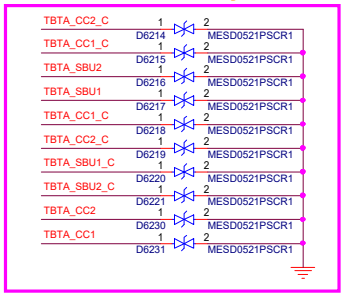
65W,20V,3.25A
130MIL



130MIL

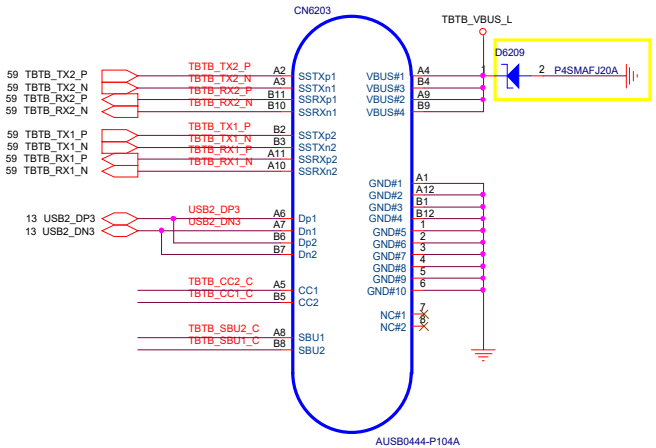


Resever for ESD debug

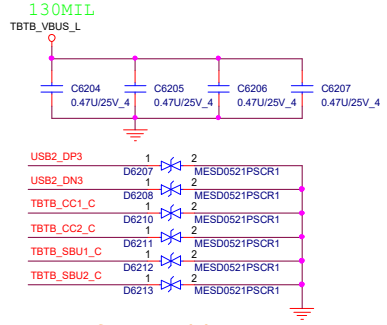


USB Type-C Port B

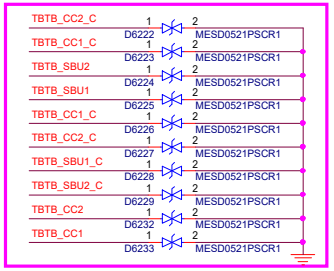
65W,20V,3.25A
130MIL

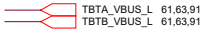


130MIL



Resever for ESD debug





PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB TYPE-C_Port A,B	3A

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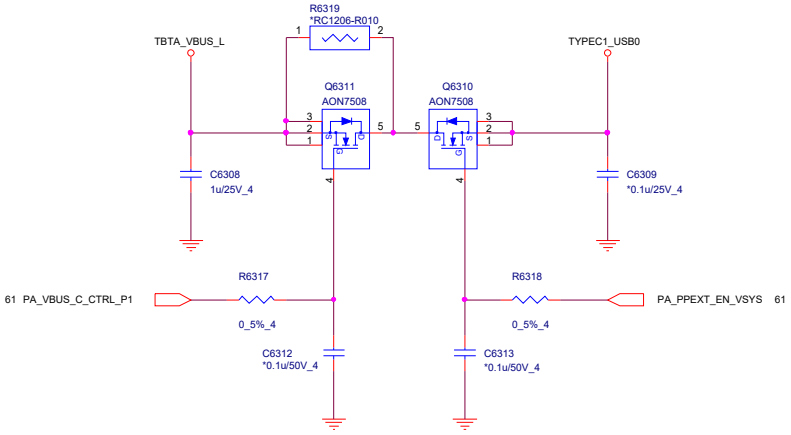
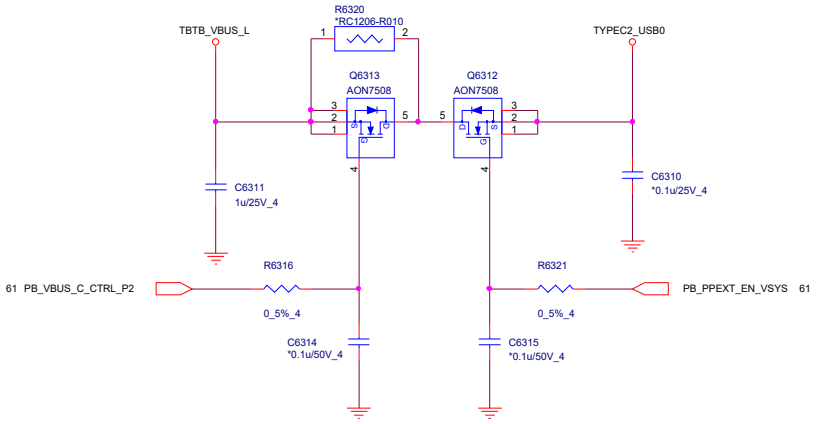
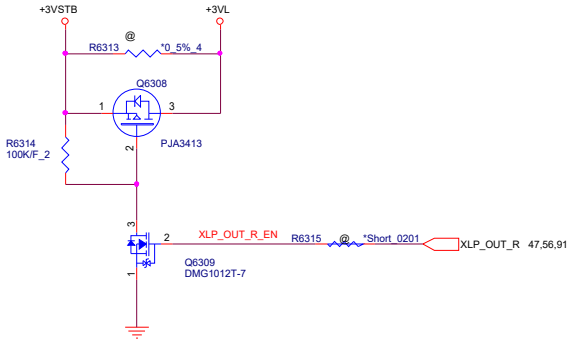




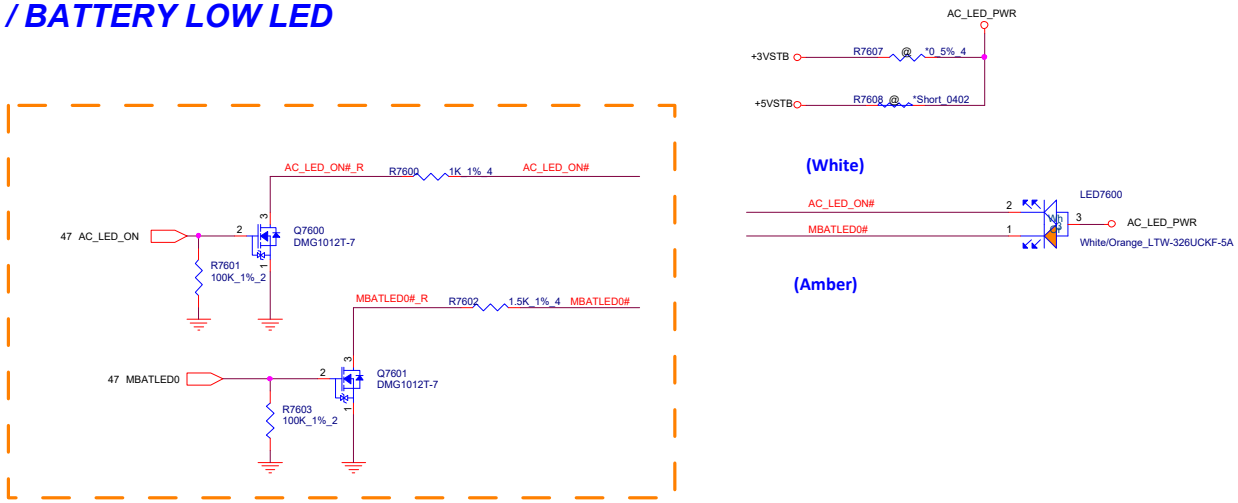


TBTA_VBUS_L 61,62,91
TBTB_VBUS_L 61,62,91
TYPEC1_USB0 63,81,82
TYPEC2_USB0 63,81,82
TYPEC1_USB0 63,81,82
TYPEC2_USB0 63,81,82

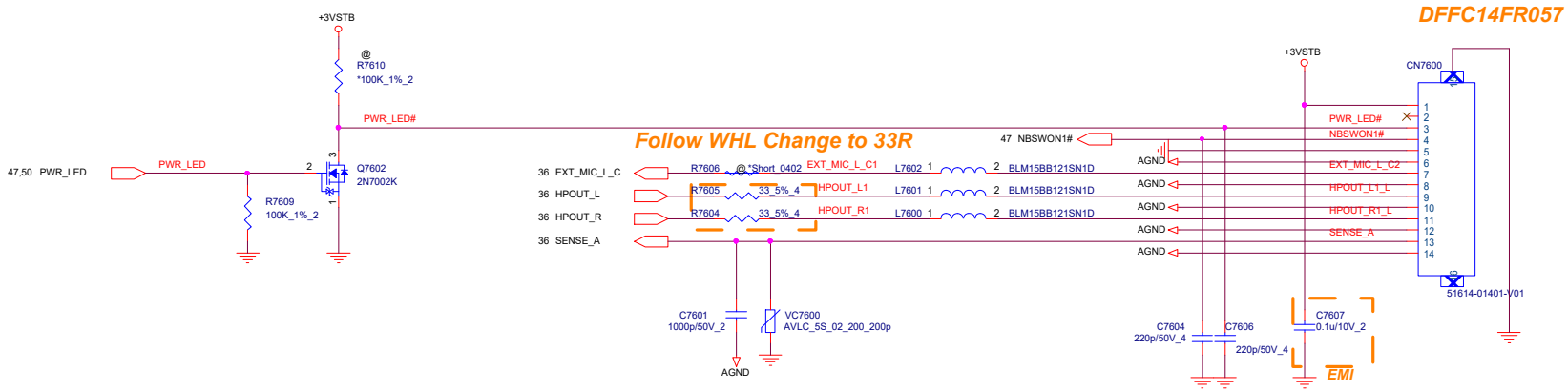
for LPMused

	PROJECT : X3AC Quanta Computer Inc.	
Size Custom	Document Number **TYPE C S/W EE**	Rev 3A
Date: Wednesday, October 07, 2020	Sheet 42 of 57	

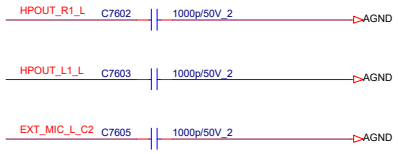
AC_IN / BATTERY LOW LED



Audio Jack & Power Button Daughter Board



EMI



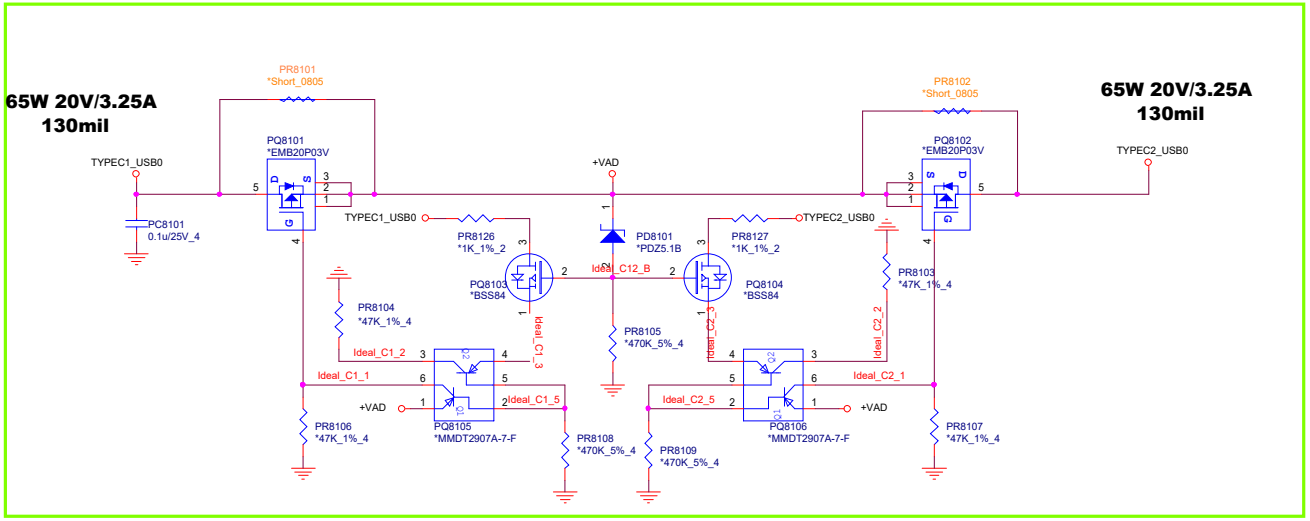
PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AC IN LED+ Audio board	3A

Date: Wednesday, October 07, 2020 | Sheet 43 of 57

For TypeC PORT1

For TypeC PORT2



remove ideal diode
2020/07/21

PROJECT : X3AC Quanta Computer Inc.		
Size: Custom	Document Number: TYPEC load switch MOSFET	Rev: 3A
Date: Wednesday, October 07, 2020	Sheet: 46 of 57	

HERO13.3 ICL_UMA 0423

6V 10A ; Only supply 65W;OCP limit to 90W

PL12 PL13 near PR51

Default setting

	Ra
3cell	105K
4cell	316K

Minimum: 3.93V

Ra

4S1P 61Whr

Place this cap close to EC

Place this cap close to EC

2019/5/18 updated

Dual

VDD=5V

+VIN 34,37,78,80,83,84,87,88,92
+3VSTB 47,48,50,56,58,61,63,76,78,91
+BAT_RTC 12,14,16,47,50,90,91
BATT+STB 91
+3VPCU 10,14,15,16,41,42,83,90,91

PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger	3A
Date: Wednesday, October 07, 2020	Sheet 47 of 57	

+3VS5 10,12,15,16,34,41,42,47,53,56,58,59,84,85,86,88,89,90,92
+3VSTB 47,48,50,56,58,61,63,76,78,82,91
+5VPCU 61,89
+VIN 34,37,78,80,82,84,87,88,92
+5VS5 86,87,88,89,90,91
+3VPCU 10,14,15,16,41,42,82,90,91
HWPG

+3.3 Volt +/- 5%
EDP:6A
EDP:8A

+5 Volt +/- 5%
TDC:7A
EDP:9A

2019/8/5 update
2019/11/07 update
2019/4/1 update

Do Not add test pad on LDO pin
Do Not add test pad on VCC & LDO pin

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

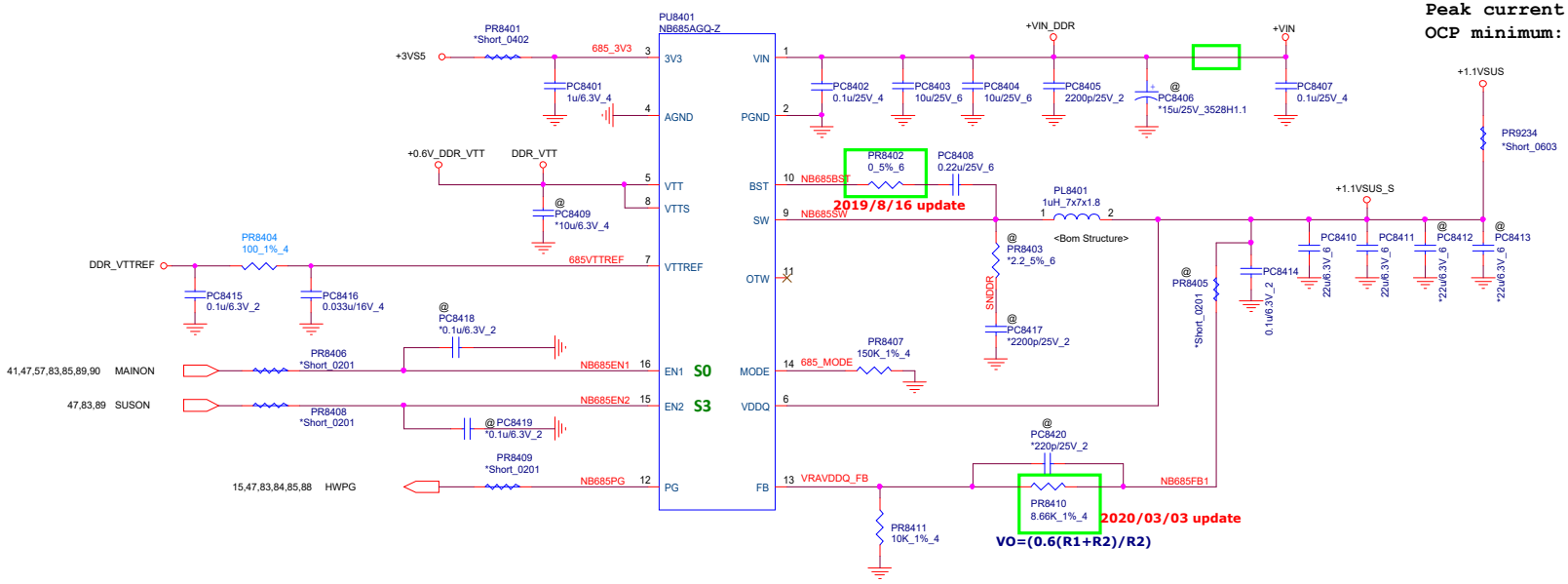
Default setting

PROJECT : X3AC
Quanta Computer Inc.

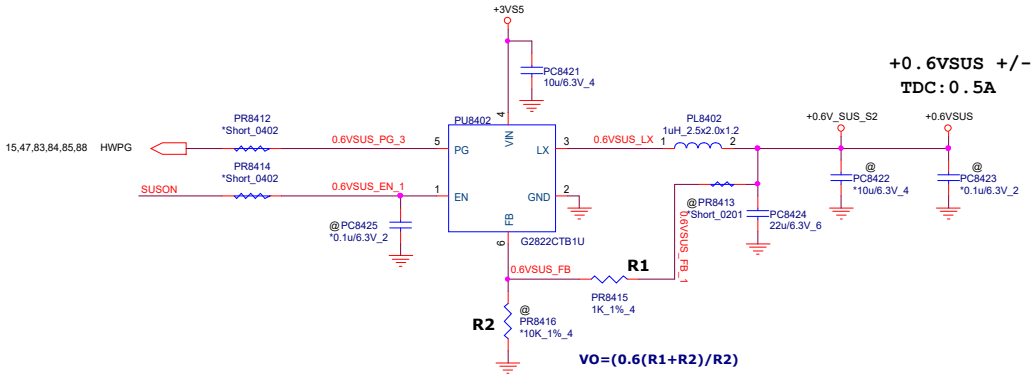
Size	Document Number	Rev
Custom	+3/5VS5(RT6256B/RT6258C)	3A

Date: Wednesday, October 07, 2020 Sheet 48 of 57

+1.1VSUS +/-5%
Continuous current: 8A
Peak current: 10A
OCP minimum: 12A



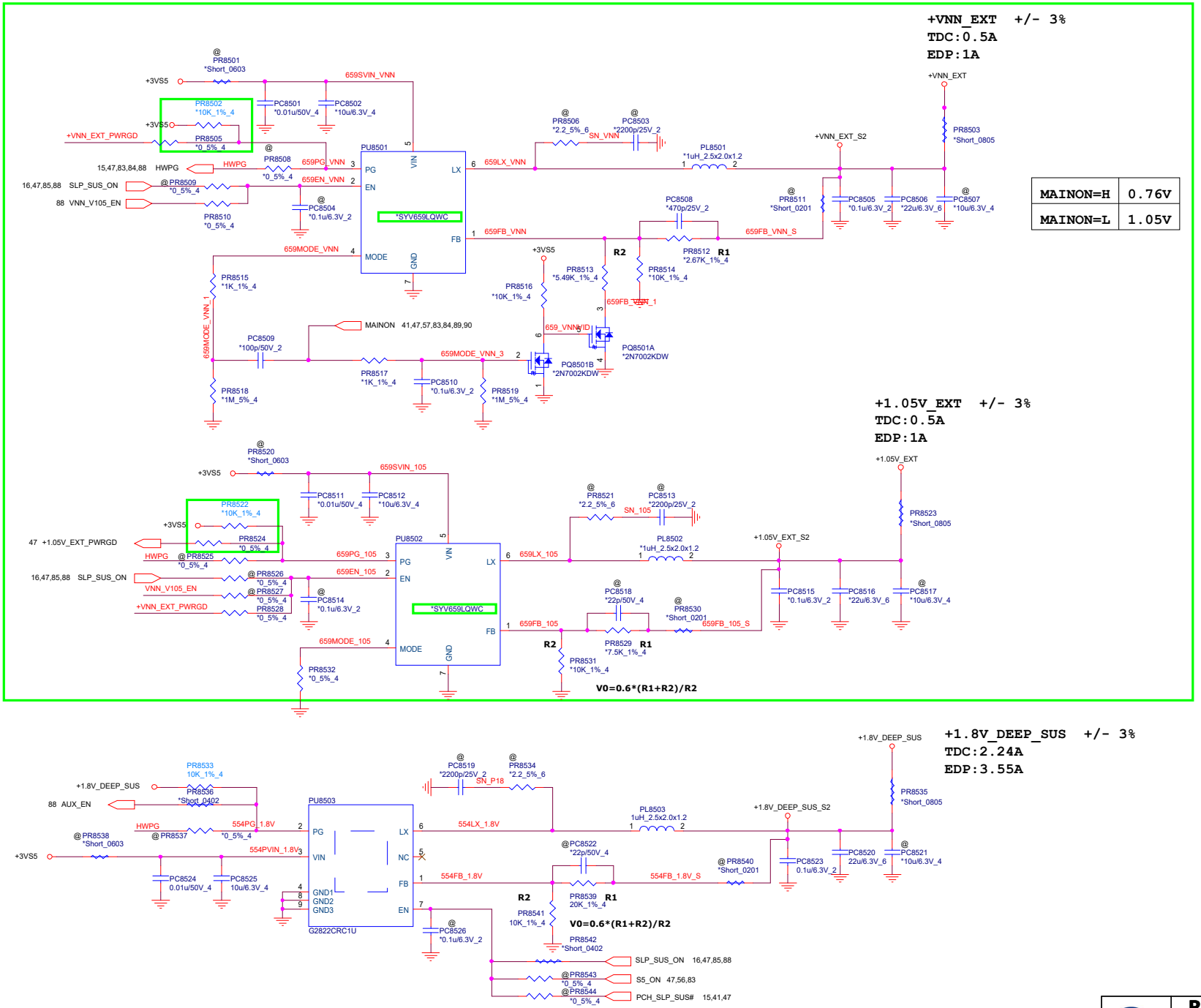
+0.6VSUS +/- 5%
TDC:0.5A



PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
	LPDDR4X (NB685A)	3A

Date: Wednesday, October 07, 2020 | Sheet 49 of 57


+VNN_EXT +/- 3%
TDC:0.5A
EDP:1A
MAINON=H 0.76V
MAINON=L 1.05V
+1.05V_EXT +/- 3%
TDC:0.5A
EDP:1A
V0=0.6*(R1+R2)/R2
+1.8V_DEEP_SUS +/- 3%
TDC:2.24A
EDP:3.55A
V0=0.6*(R1+R2)/R2
PU8501
PU8502
PU8503
*SYV659LQWC
G2822CRC1U
+3VS5
+VNN_EXT
+1.05V_EXT
+1.8V_DEEP_SUS
MAINON 41,47,57,83,84,89,90
SLP_SUS_ON 16,47,85,88
S5_ON 47,56,83
PCH_SLP_SUS# 15,41,47
PROJECT : X3AC
Quanta Computer Inc.
+VNN_EXT/+1.8V_DEEP_SUS
Wednesday, October 07, 2020
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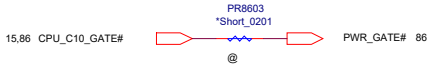
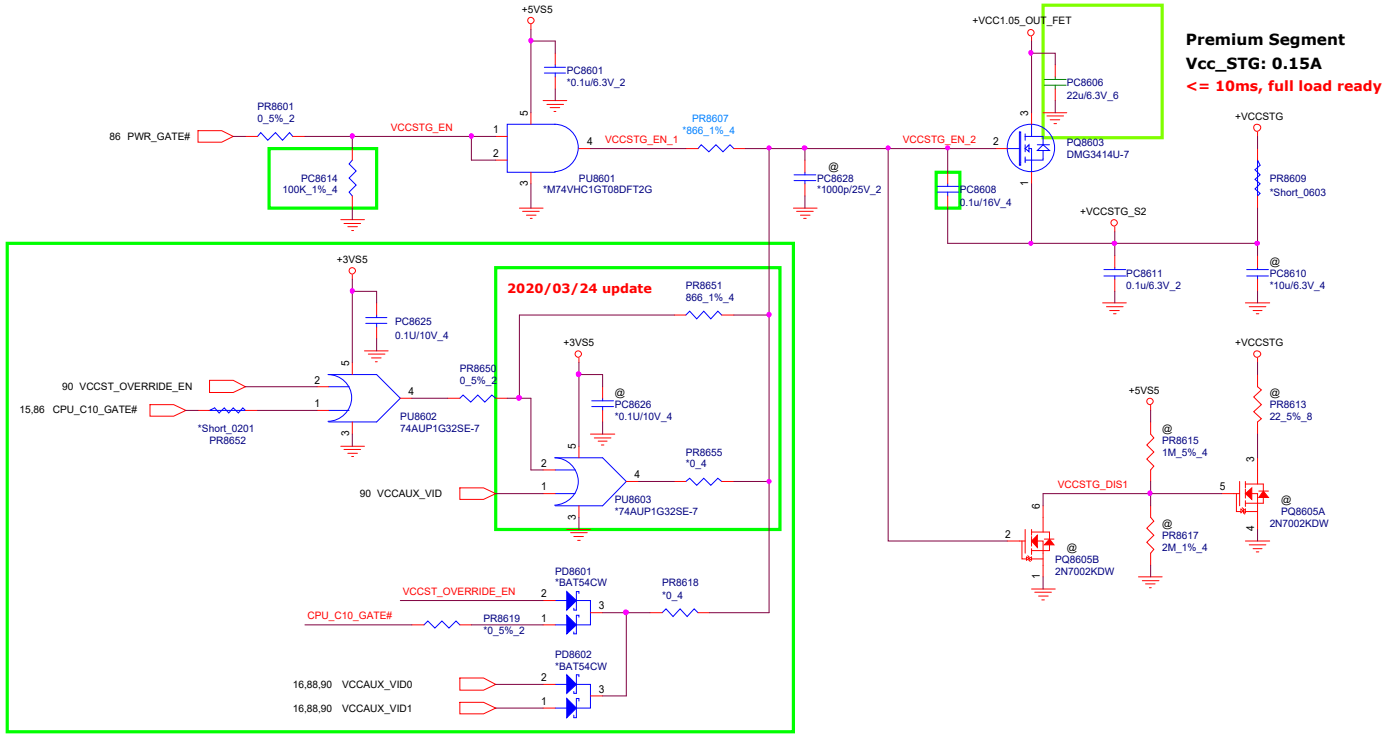
Premium Segment
ICL U42

Volume Segment
ICL U42



2019/11/14 update

Premium Segment
Vcc_STG: 0.15A
<= 10ms, full load ready



2020/03/24 updated

PROJECT : X3AC Quanta Computer Inc.		
Size: Custom	Document Number: +VCCST/VCCSTG/+VCC1P8A	Rev: 3A
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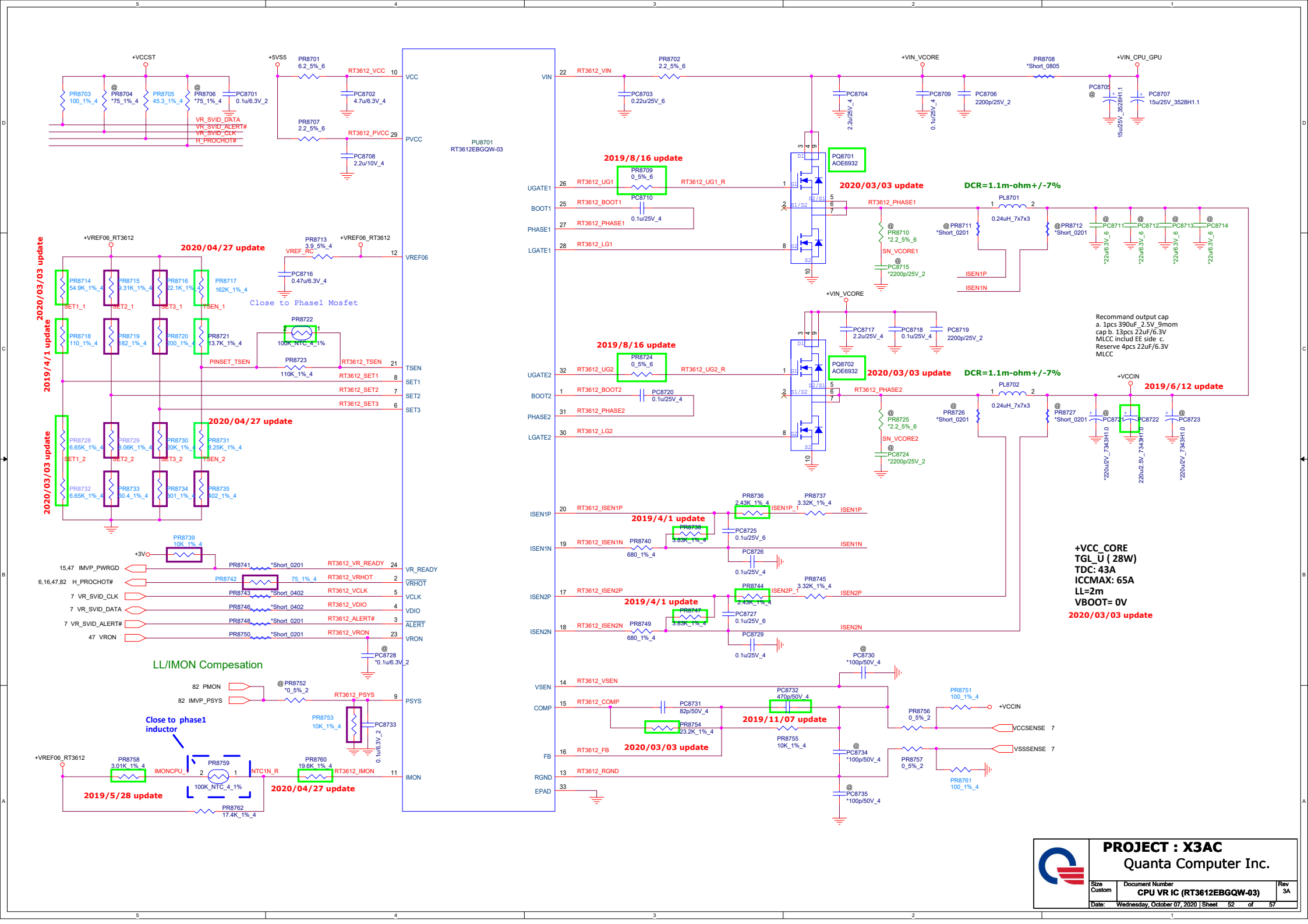
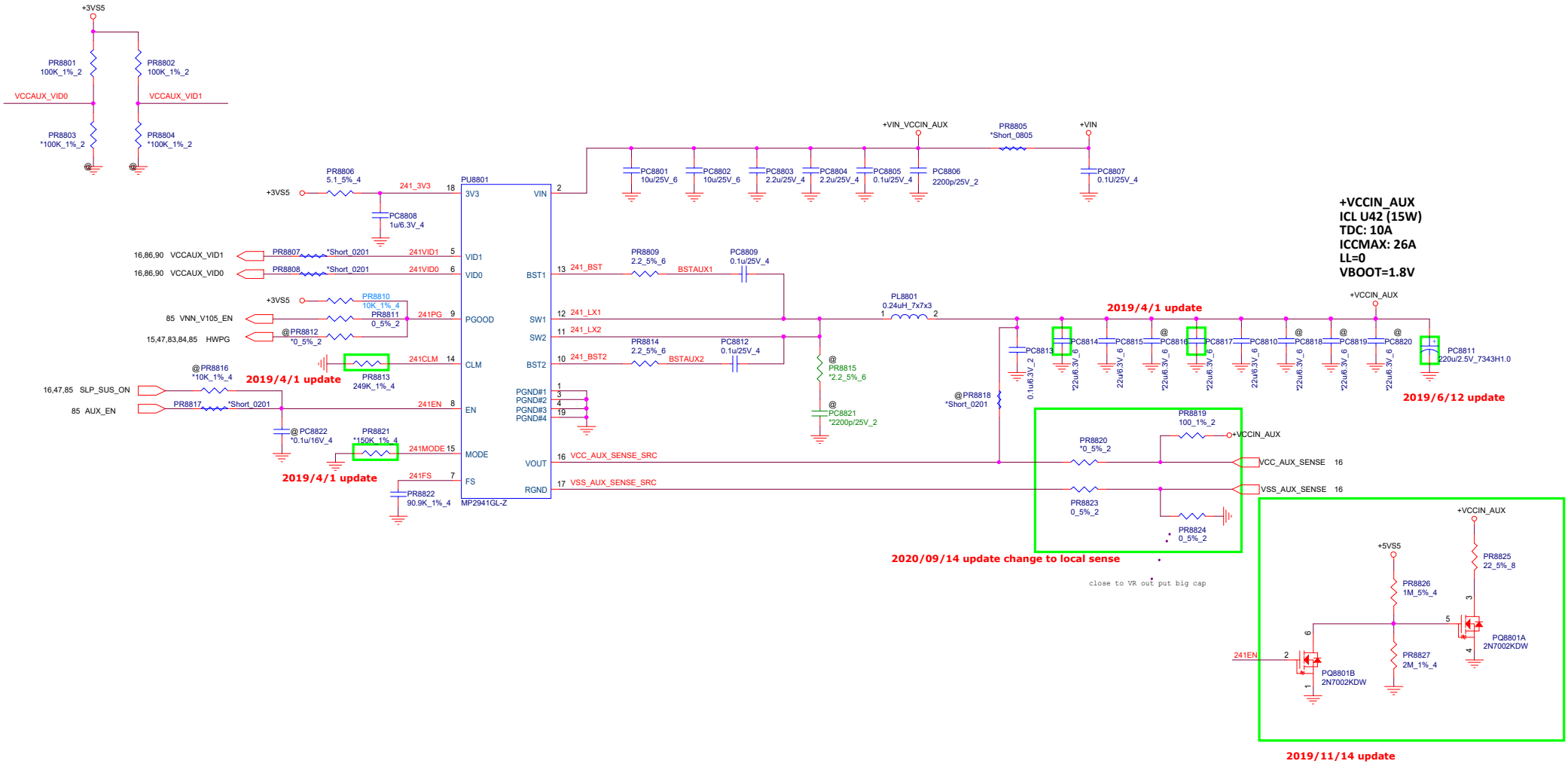

PU8701
RT3612EBGQW-03
VCC
PVCC
TSEN
SET1
SET2
SET3
VR_READY
VRHOT
VCLK
VDIO
ALERT
VRON
PSYS
IMON
VREF06
VIN
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
LGATE2
ISEN1P
ISEN1N
ISEN2P
ISEN2N
VSEN
COMP
FB
RGND
EPAD
+VCCST
+5VS5
+VREF06_RT3612
+3V
+VIN_VCORE
+VIN_CPU_GPU
+VCCIN
2019/8/16 update
2020/03/03 update
DCR=1.1m-ohm+/-7%
2020/04/27 update
2019/4/1 update
2020/03/03 update
2019/4/1 update
2019/11/07 update
2020/03/03 update
2020/04/27 update
2019/5/28 update
2019/6/12 update
Close to Phase1 Mosfet
Close to phase1 inductor
LL/IMON Compesation
Recommand output cap
a. 1pcs 390uF_2.5V_9mom
cap b. 13pcs 22uF/6.3V
MLCC includ EE side c.
Reserve 4pcs 22uF/6.3V
MLCC
+VCC_CORE
TGL_U (28W)
TDC: 43A
ICCMAX: 65A
LL=2m
VBOOT= 0V
2020/03/03 update
PROJECT : X3AC
Quanta Computer Inc.
CPU VR IC (RT3612EBGQW-03)
Size Custom
Rev 3A
Date: Wednesday, October 07, 2020
Sheet 52 of 57



PROJECT : X3AC

Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCCIN_AUX IC (MP2941)	3A

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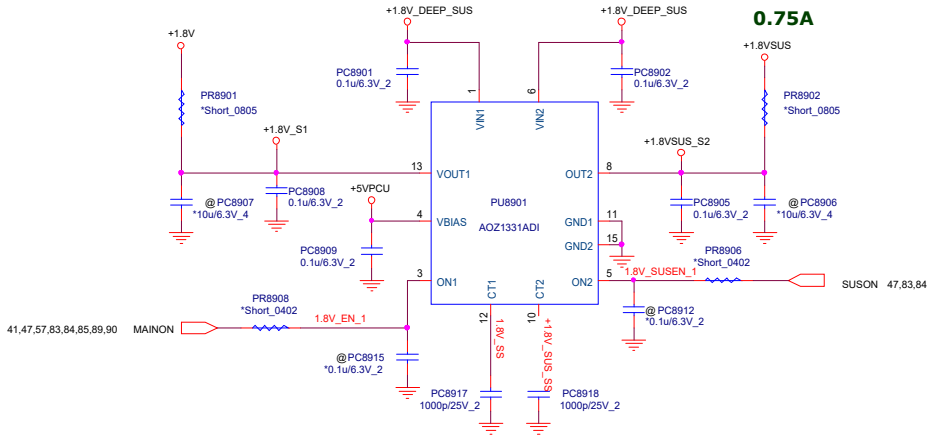
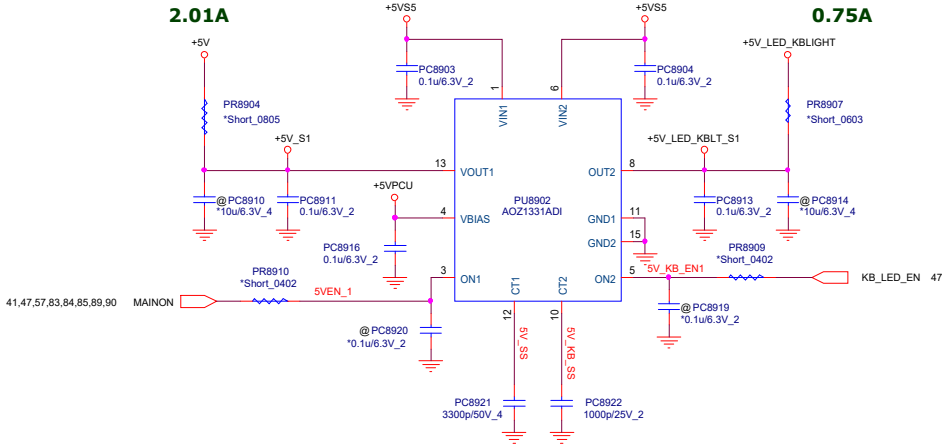
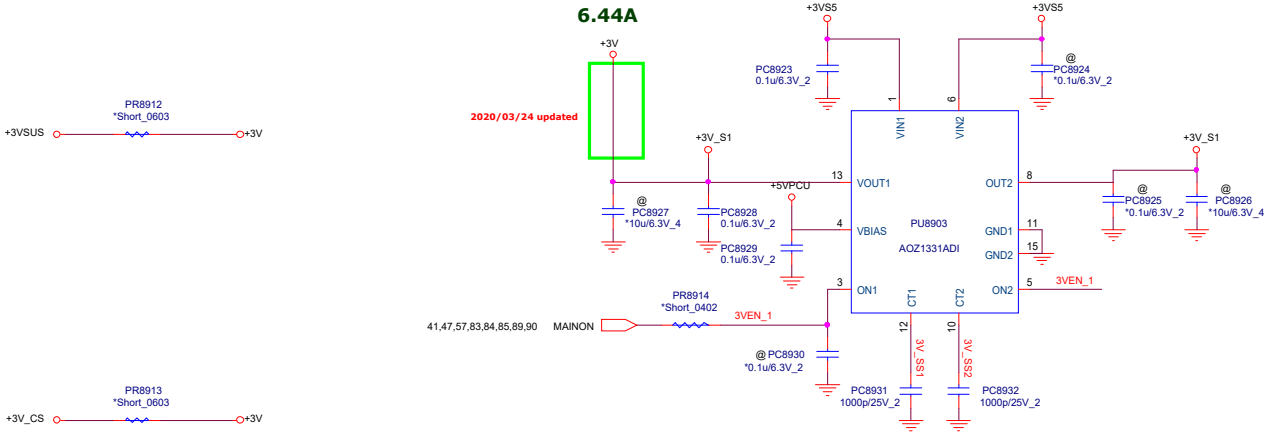




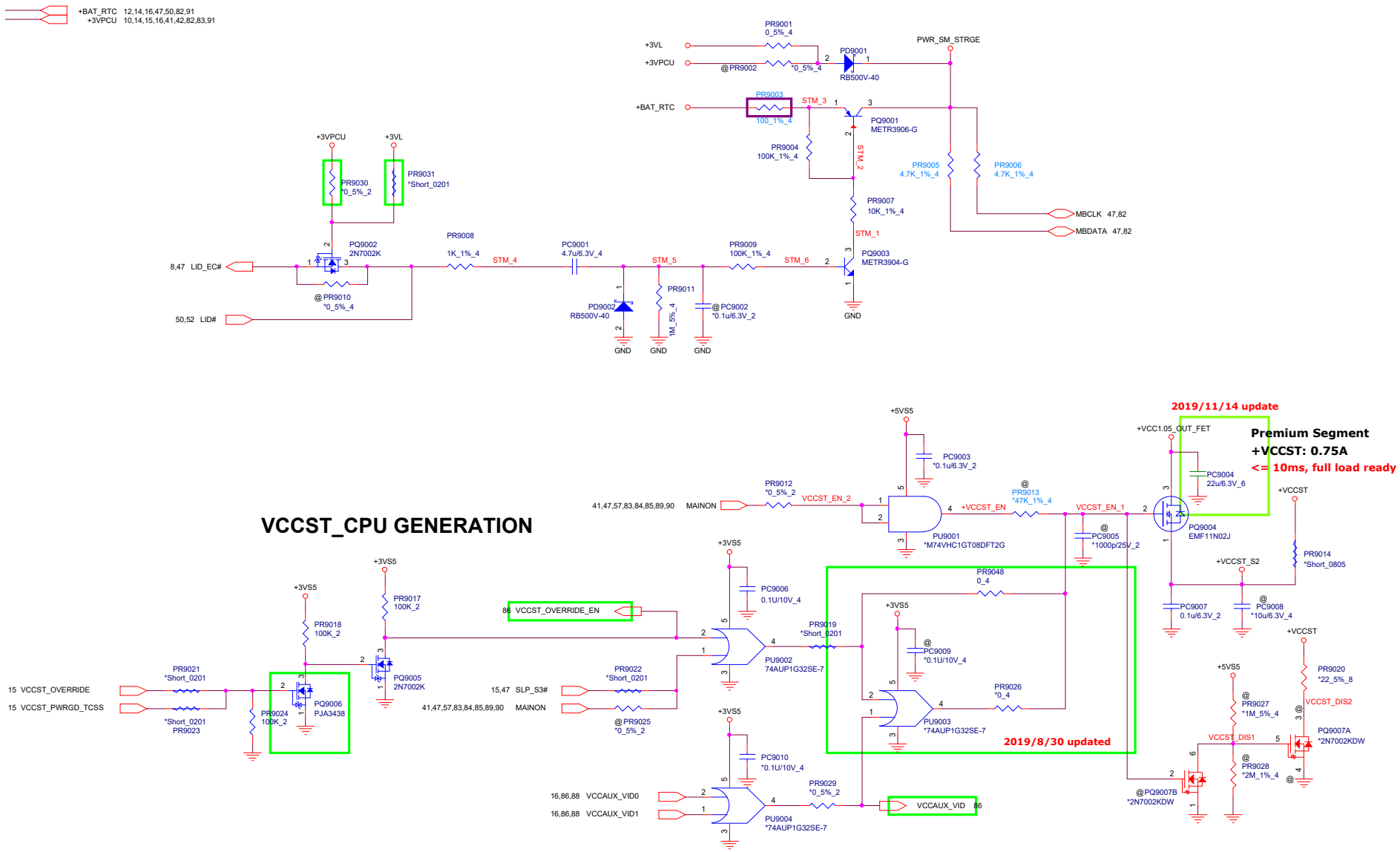


PROJECT : X3AC

Quanta Computer Inc.

Size	Document Number	Rev
	Load switch IC(APL3523A)	3A

Date: Wednesday, October 07, 2020 | Sheet 54 of 57

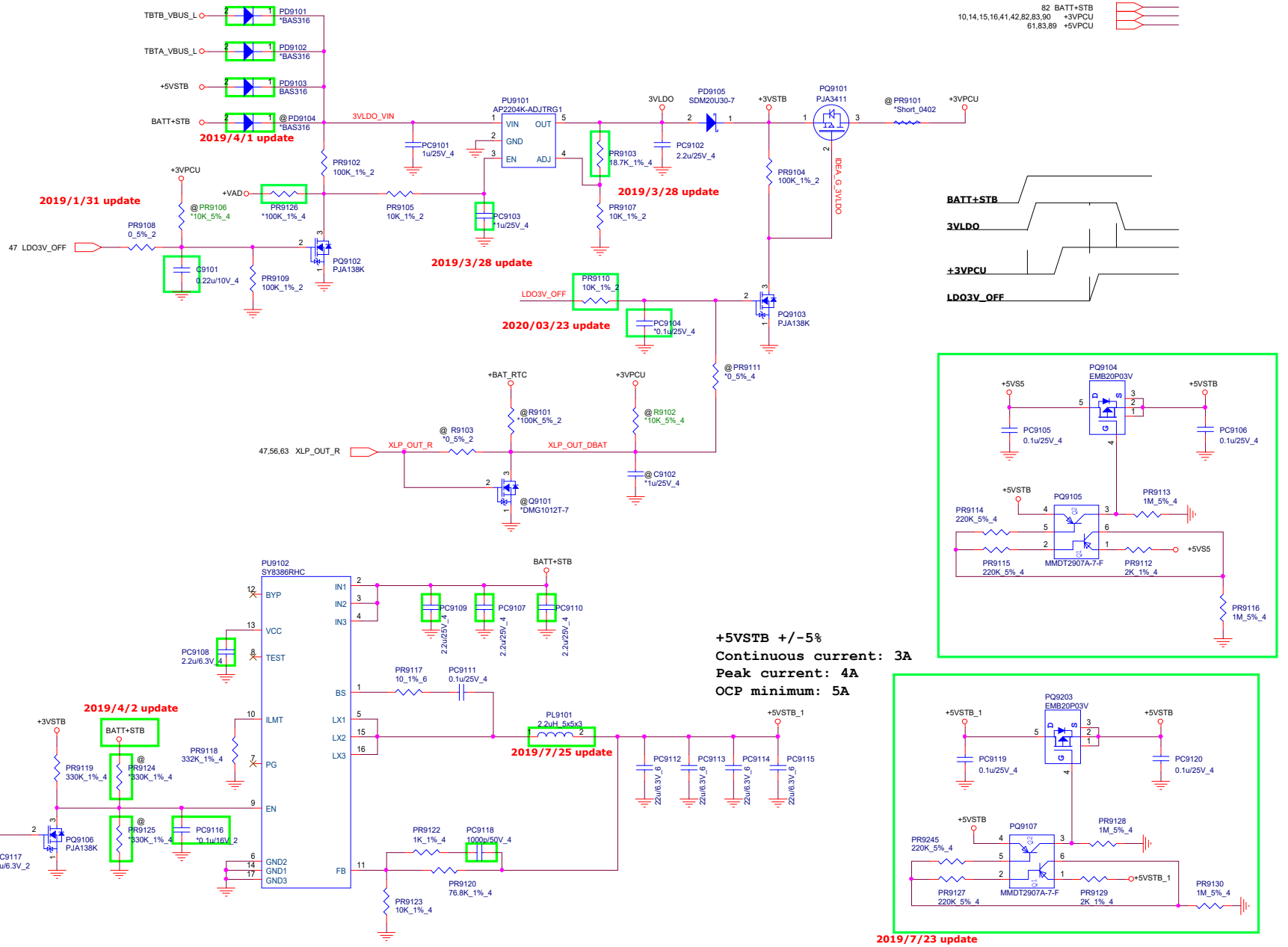


PROJECT : X3AC

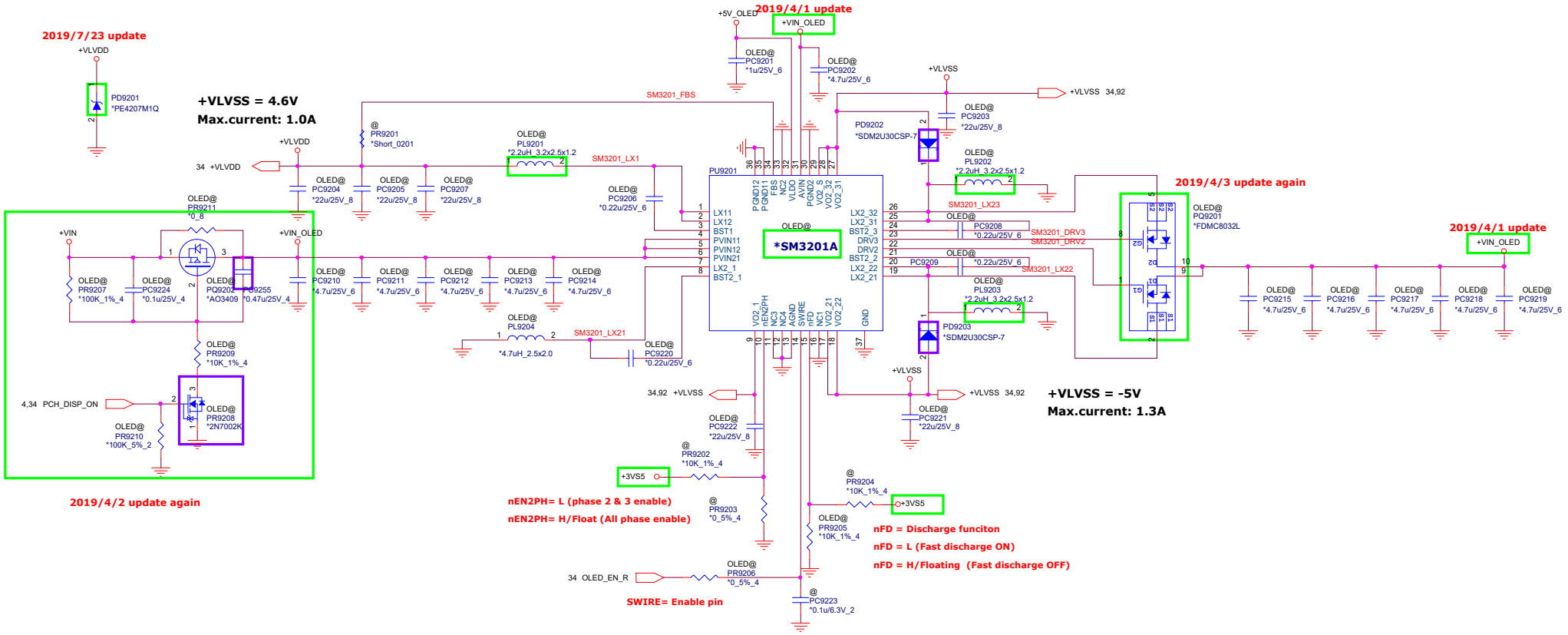
Quanta Computer Inc.

Size	Document Number	Rev
Custom	STORAGE MODE	3A

Date: Wednesday, October 07, 2020 Sheet 55 of 57



PROJECT : X3AC	
Quanta Computer Inc.	
Size: Custom	Document Number: Low Power Mode
Rev: 3A	
Date: Wednesday, October 07, 2020	Sheet 56 of 57



PROJECT : X3AC

Quanta Computer Inc.

Size	Document Number	Rev
Custom	OLED power	3A

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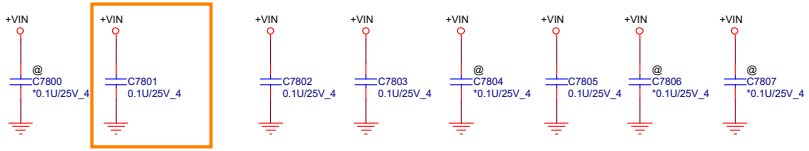
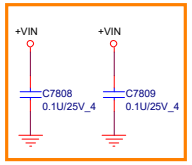
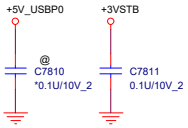
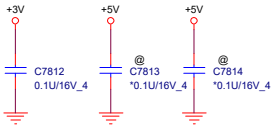
EMI CAP

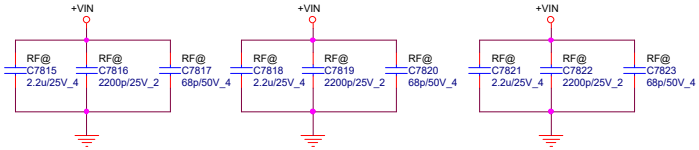


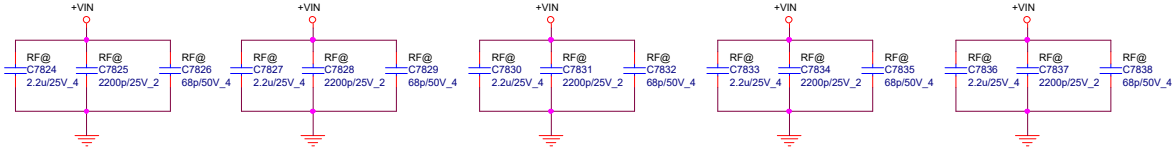


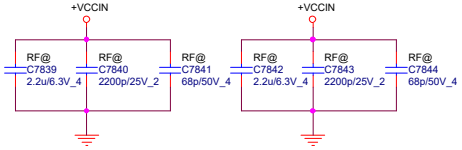


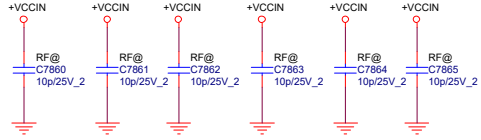


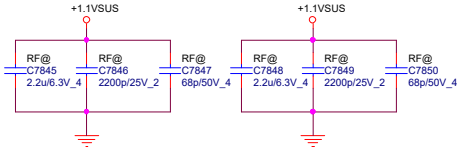
RF CAP

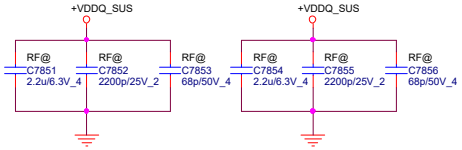


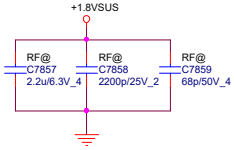


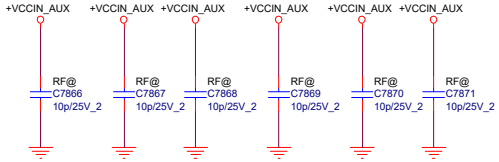












PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI / RF CAP	3A

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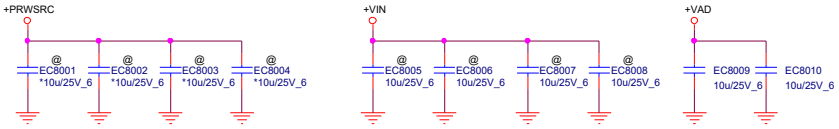

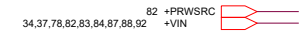

PROJECT : X3AC
Quanta Computer Inc.

Size	Document Number	Rev
	Power EMI	3A

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MODEL	REV	CHANGE LIST
X3AC MB	3A	First Release E202007-8639

Page \ Model	X3AC MB FROM	X3AC MB TO
1		3A
2		3A
3		3A
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54		3A
55		3A
56		3A
57		3A

Quanta Computer Inc.	PROJECT:X3AC	REV:3A	DOCUMENT NO.: 204	PCBA P/N: 31X3AMB0460
	APPROVED BY: Vincent Lee	DRAWING BY: Neil Chen	DATE: 2020/09/29	SHEET 1 OF 1